Balance carrier v2 · v0.9

Subsystem circuit schematics

One schematic per subsystem, in the same order as SUBSYSTEMS.pdf (block diagrams, board maps and layout checks). The KiCad schematic itself is kicad/balance_carrier/balance_carrier.pdf.

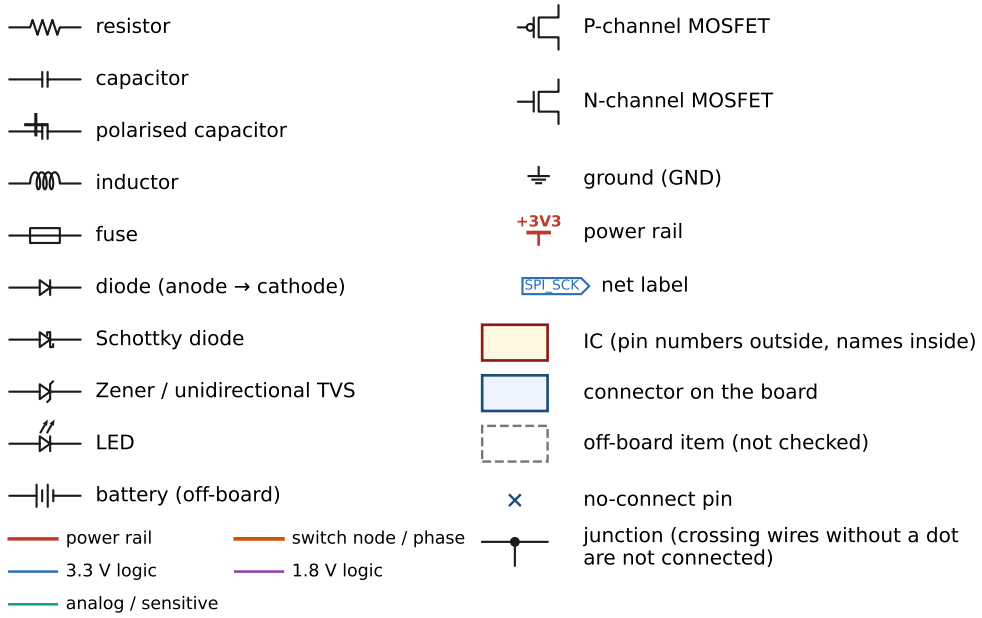
Every pin shows its datasheet name and number, taken from the KiCad symbols. Every wire, net label and power symbol is checked against the netlist: the build stops on any short, open pin or missing part.

Parts with the same net label or power symbol are connected, on this sheet or another; the last page lists the sheets each net appears on.

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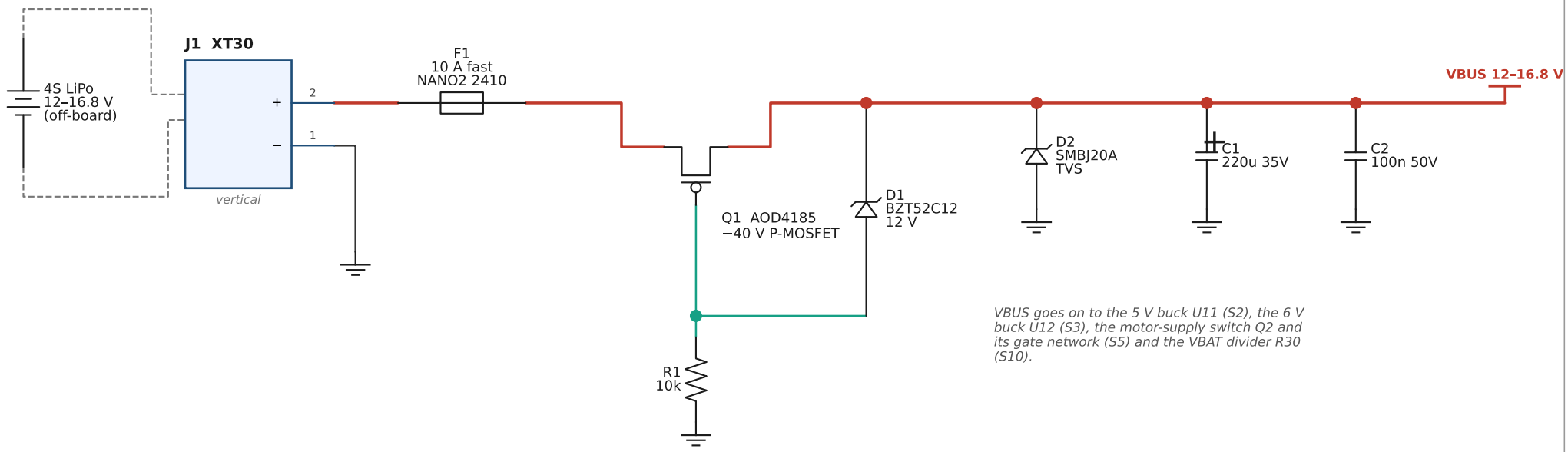
Symbol legend



Project	Balance carrier v2 (Milk-V Duo S carrier)
Sheet	**Cover and symbol legend**
Revision	v0.9
Source	hardware/kicad/balance_carrier (netlist + symbols)
Generated by	tools/hardware/build_circuits.py
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S1 Power entry and reverse-polarity protection

Brings the 4S pack in through the XT30, fuses it, blocks a reversed battery with a P-MOSFET and clamps transients. Its output, VBUS, feeds both bucks, the motor-supply switch and the battery monitor.



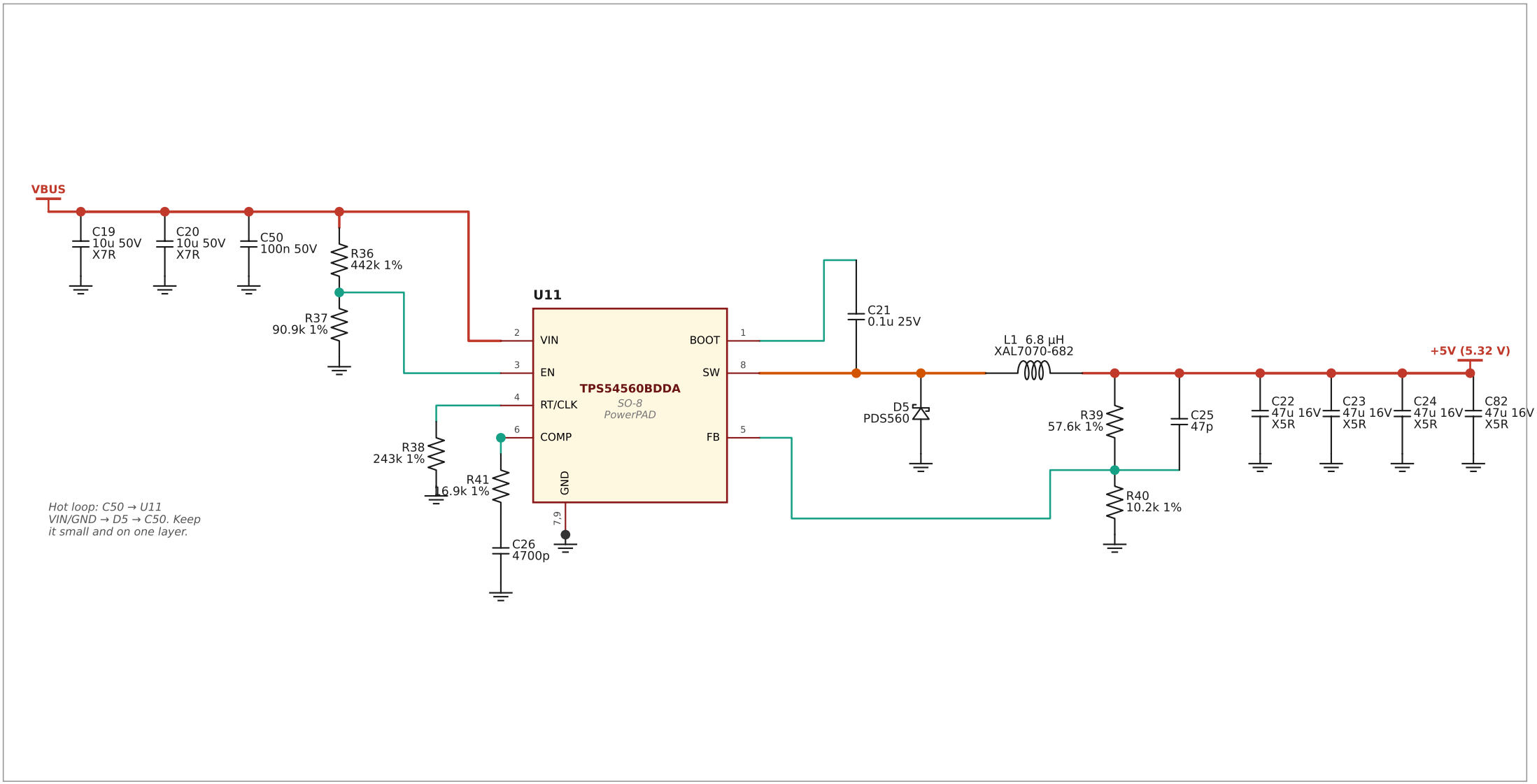
Derived values

- Q1 gate: R1 holds it at GND, so Vgs = −VBUS: −12 V to −16.8 V. D1 clamps it at −12 V, inside the AOD4185's ±20 V rating.
- Reversed pack: the gate sits at the source and the body diode blocks, so VBUS stays at 0 V.
- D2: 20 V standoff above the 16.8 V full pack, about 32 V clamp; C1 is rated 35 V, every VBUS ceramic 50 V.
- F1: 10 A against about 7.4 A worst case: both motors stalled (3 A), both servos stalled through the 6 V buck on a 12 V pack (4 A), logic (0.4 A). The VBUS accessory output (S13) adds up to its 2.5 A limit: 9.9 A with everything stalled at once, no demonstrated margin.

Project	Balance carrier v2 (Milk-V Duo S carrier)
Sheet	**S1 Power entry and reverse-polarity protection**
Revision	v0.9
Source	hardware/kicad/balance_carrier (netlist + symbols)
Generated by	tools/hardware/build_circuits.py
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S2 5 V logic rail: TPS54560B buck (U11)

Steps VBUS down to 5.32 V for the Duo S (through D3) and the 3.3 V / 1.8 V LDOs. TI's 5 V / 5 A reference design: asynchronous, 400 kHz, external PDS560 catch diode, type-II compensation.



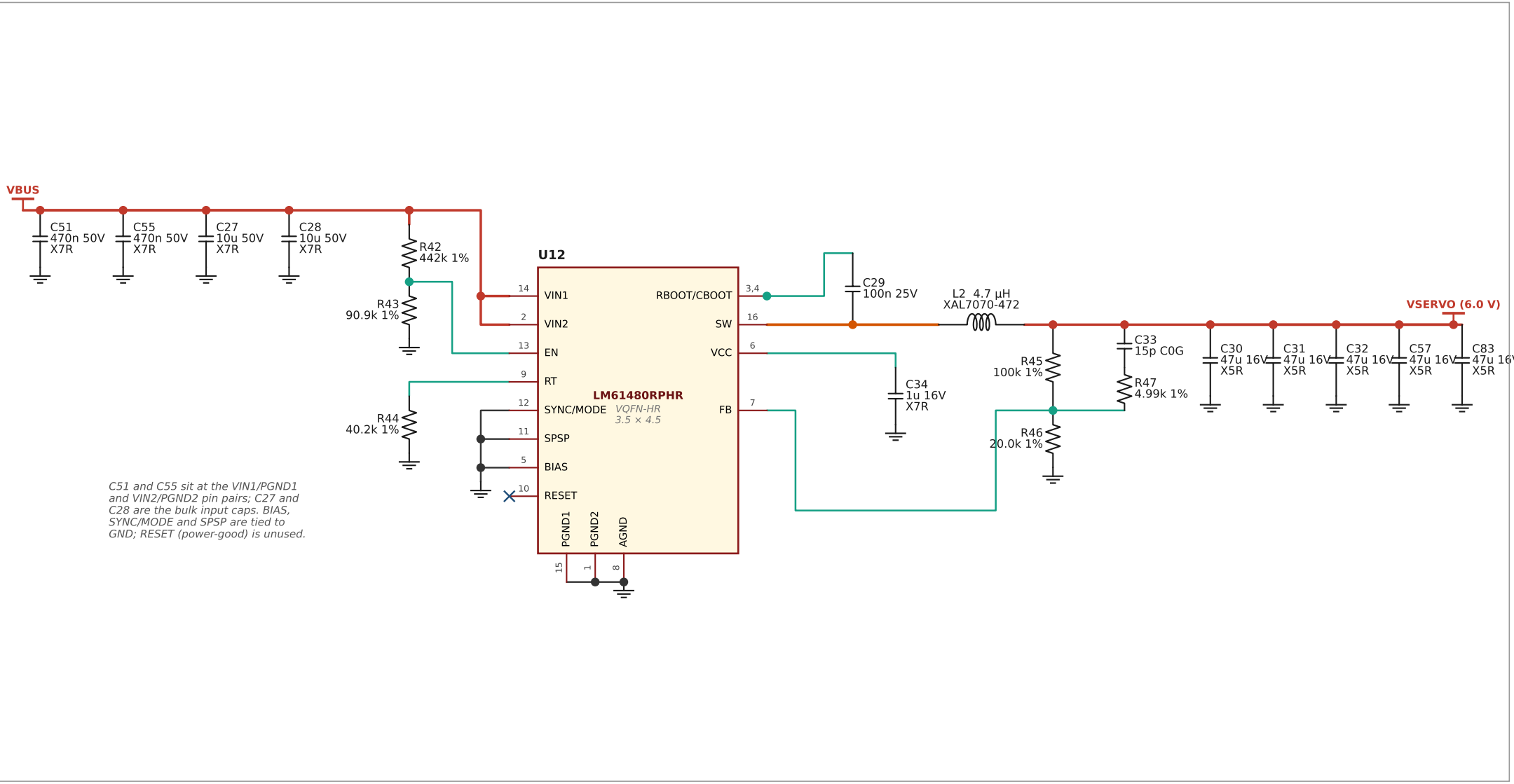
Derived values

- Vout = 0.8 V × (1 + R39/R40) = 0.8 × (1 + 57.6k/10.2k) = 5.32 V; VSYS is one SS34 drop lower, about 4.9 V.
- fsw = (101756 / RT[kΩ])^(1/1.008) = 399 kHz (TPS54560 datasheet).
- UVLO start = 1.2 V × (1 + R36/R37) − 1.2 µA × R36 = 6.5 V, below a flat 4S pack (12 V).
- Inductor ripple at 16.8 V in: ΔI = (Vin − Vout)·Vout / (Vin·L·f) = 1.34 A p-p (load about 1.2 A, plus up to 0.5 A through the 5 V accessory output; U11 limit 5 A).

Project	Balance carrier v2 (Milk-V Duo S carrier)
Sheet	**S2 5 V logic rail: TPS54560B buck (U11)**
Revision	v0.9
Source	hardware/kicad/balance_carrier (netlist + symbols)
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S3 6 V servo rail: LM61480 synchronous buck (U12)

Steps VBUS down to 6.0 V at up to 8 A for the two DS3240 knee servos. Synchronous, 400 kHz, internal compensation with a feed-forward RC, values from TI SNVSBZ4A section 9.2.



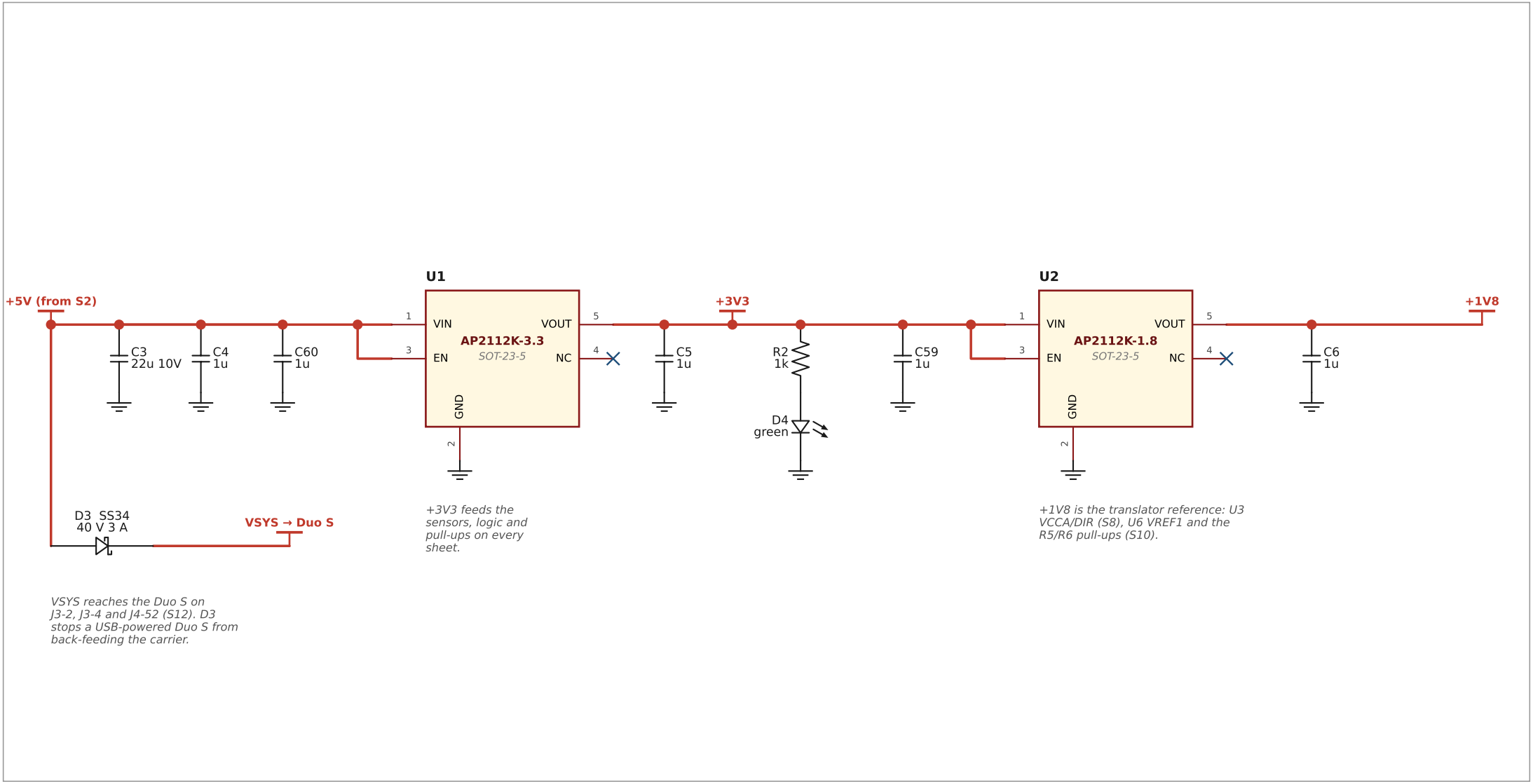
Derived values

- Vout = 1.0 V × (1 + R45/R46) = 1.0 × (1 + 100k/20k) = 6.00 V.
- Precision-EN UVLO: on at 1.263 V × (1 + R42/R43) = 7.4 V.
- Inductor ripple at 16.8 V in: ΔI = (Vin − Vout)·Vout / (Vin·L·f) = 2.05 A p-p; XAL7070-472: 15.2 A at 30% L reduction (25°C), versus 13.8 A typical / 15.6 A maximum IC limit; hot/fault margin remains to be verified.
- Two stalled DS3240s draw about 7 A. IC rating is 8 A; usable continuous and burst current require thermal/load measurements on this PCB.

Project	Balance carrier v2 (Milk-V Duo S carrier)
Sheet	**S3 6 V servo rail: LM61480 synchronous buck …**
Revision	v0.9
Source	hardware/kicad/balance_carrier (netlist + symbols)
Generated by	tools/hardware/build_circuits.py
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S4 Logic rails: VSYS feed, 3.3 V and 1.8 V LDOs

Feeds the Duo S from the 5 V buck through a Schottky (so a USB-C supply on the Duo cannot back-feed the carrier), and makes the 3.3 V logic/sensor rail and the 1.8 V translator reference.



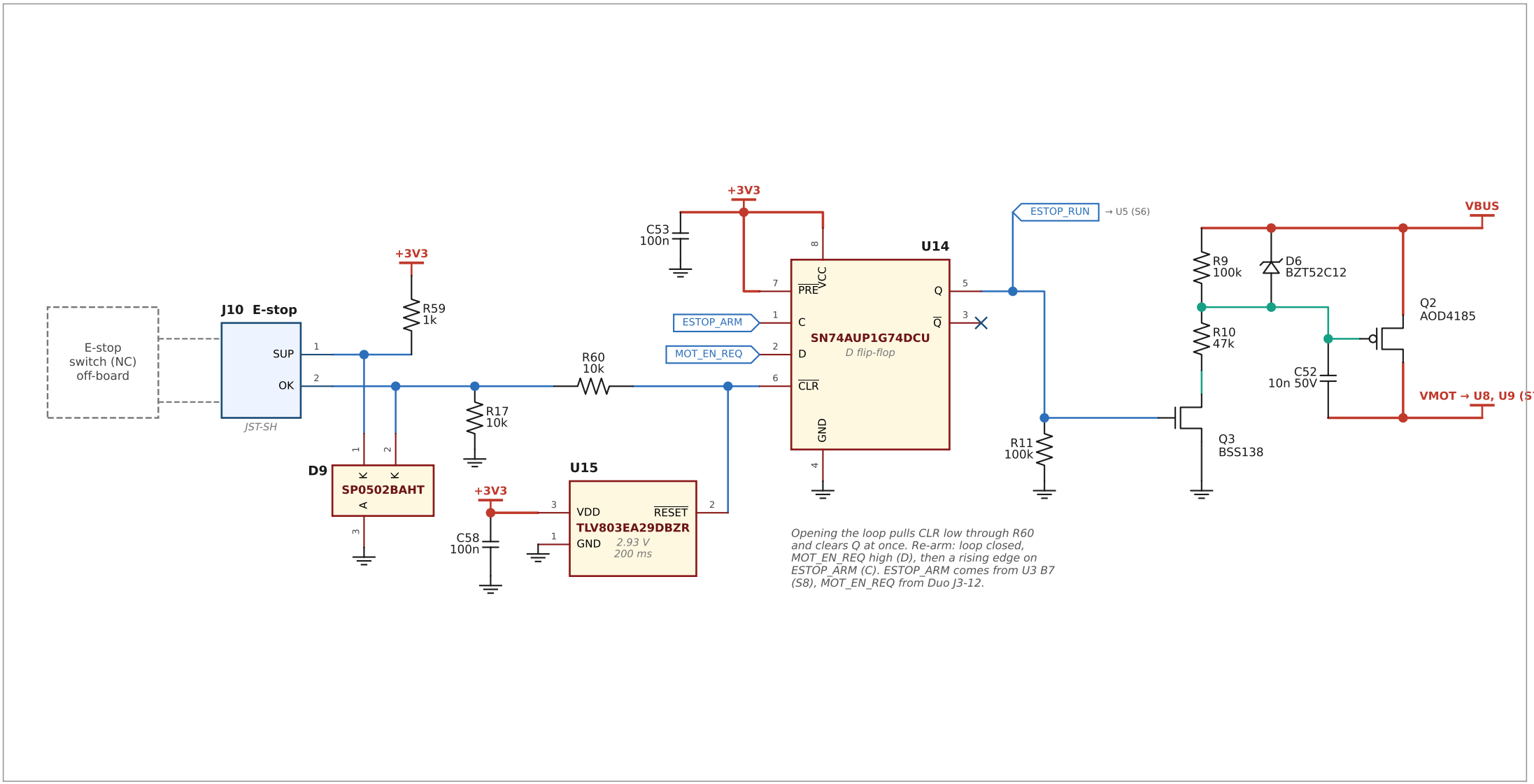
Derived values

- VSYS ≈ 5.32 V − 0.45 V (SS34 at about 1 A) ≈ 4.9 V at the Duo S.
- U1: (5.32 − 3.3) V × about 90 mA ≈ 0.18 W in a SOT-23-5. U2: (3.3 − 1.8) V × <5 mA, negligible.
- Power LED: (3.3 − 2.0) V / 1k ≈ 1.3 mA.

Project	Balance carrier v2 (Milk-V Duo S carrier)
Sheet	**S4 Logic rails: VSYS feed, 3.3 V and 1.8 V LDOs**
Revision	v0.9
Source	hardware/kicad/balance_carrier (netlist + symbols)
Generated by	tools/hardware/build_circuits.py
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S5 E-stop latch and motor-supply switch

A normally-closed E-stop loop clears a D flip-flop the instant it opens. The latch drives the high-side P-MOSFET that makes VMOT for both motor drivers, so an open loop removes motor power in hardware.



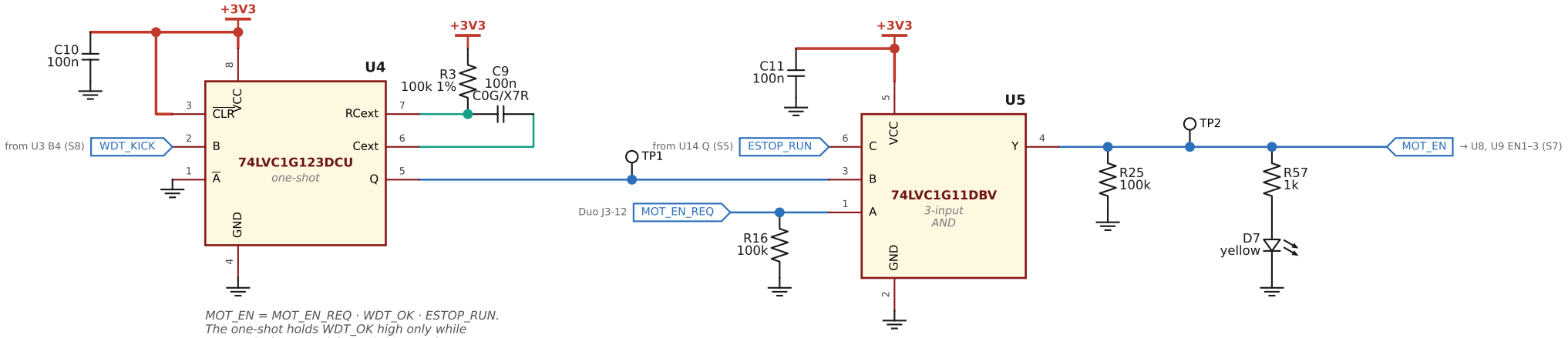
Derived values

- Q2 on: Vgs = −VBUS × R9/(R9 + R10) = −8.2 V at 12 V, −11.4 V at 16.8 V; D6 clamps at −12 V for transients.
- Loop current 0.30 mA; ESTOP_OK sits at 3.3 V × R17/(R59 + R17) = 3.0 V while closed.
- CLR is asynchronous: opening the loop drops ESTOP_RUN at once, and a bouncing switch cannot set it again.
- C52 makes Q2 a Miller ramp of roughly 30 V/ms, so the DRV8313 bulk caps charge softly; R9 turns it off in about 2 ms; VMOT rail decay is a separate measurement.

Project	Balance carrier v2 (Milk-V Duo S carrier)
Sheet	**S5 E-stop latch and motor-supply switch**
Revision	v0.9
Source	hardware/kicad/balance_carrier (netlist + symbols)
Generated by	tools/hardware/build_circuits.py
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S6 Motor-enable safety chain: watchdog and AND gate

MOT_EN = MOT_EN_REQ AND WDT_OK AND ESTOP_RUN drives every DRV8313 enable pin. WDT_OK comes from a retriggerable one-shot the control loop must keep kicking, so a hung core disables the bridges within about 10 ms without any software involved.



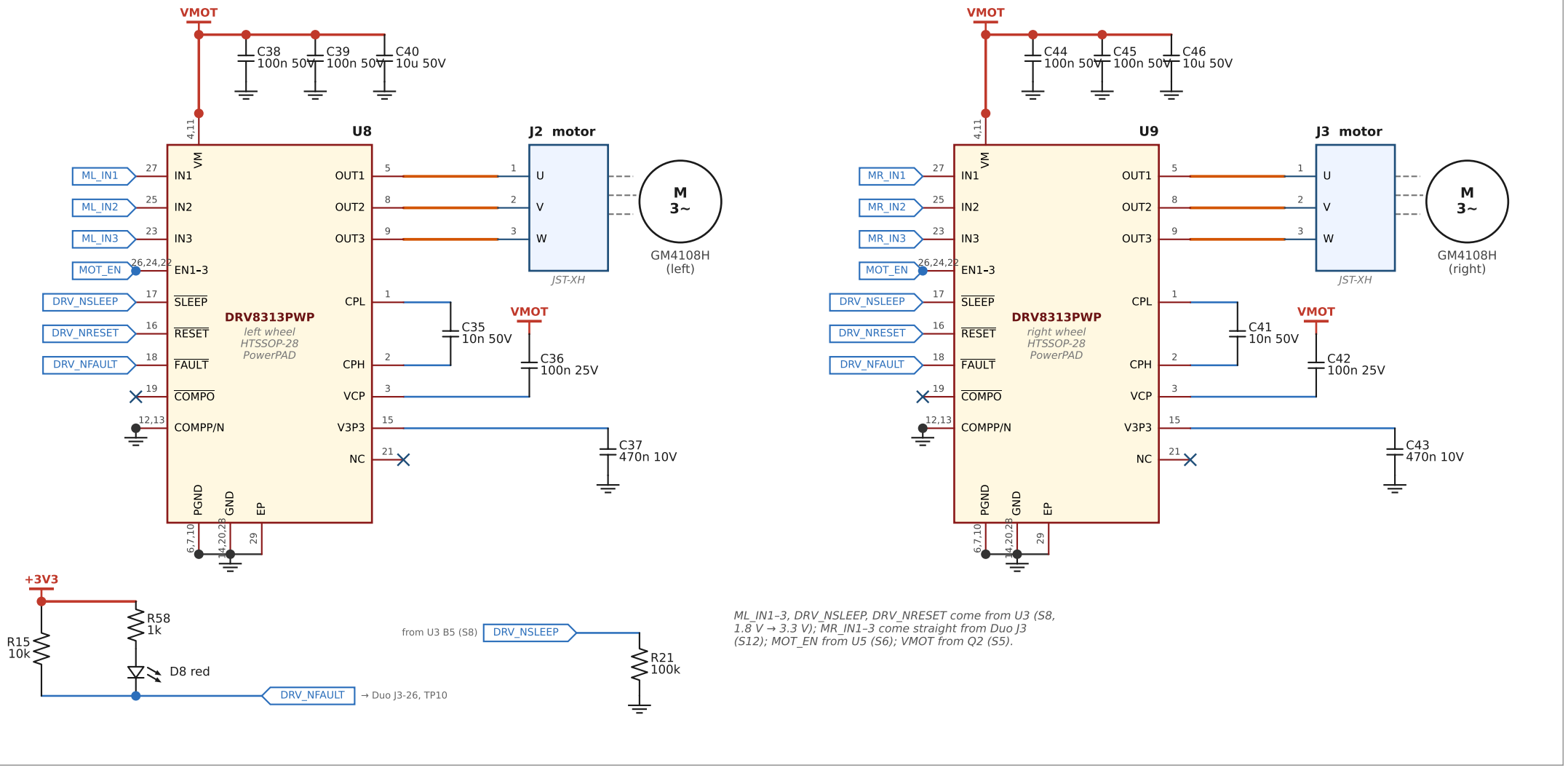
Derived values

- One-shot width tw ≈ K·R3·C9 with K ≈ 1: 10 ms, twice the 5 ms kick period at 400 Hz.
- Edge-triggered, so a core stuck with WDT_KICK high or low both time out.
- LED D7: (3.3 − 2.0) V / 1k ≈ 1.3 mA from MOT_EN.
- Pull-downs on MOT_EN_REQ and MOT_EN keep the bridges off while the Duo S boots.

Project	Balance carrier v2 (Milk-V Duo S carrier)
Sheet	**S6 Motor-enable safety chain: watchdog and …**
Revision	v0.9
Source	hardware/kicad/balance_carrier (netlist + symbols)
Generated by	tools/hardware/build_circuits.py
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S7 Wheel drivers: 2 × DRV8313 three-phase bridges

Each DRV8313 drives one GM4108H gimbal motor with three PWM half-bridges for FOC. VMOT comes from the E-stop switch (S5); the enables come from the safety chain (S6).



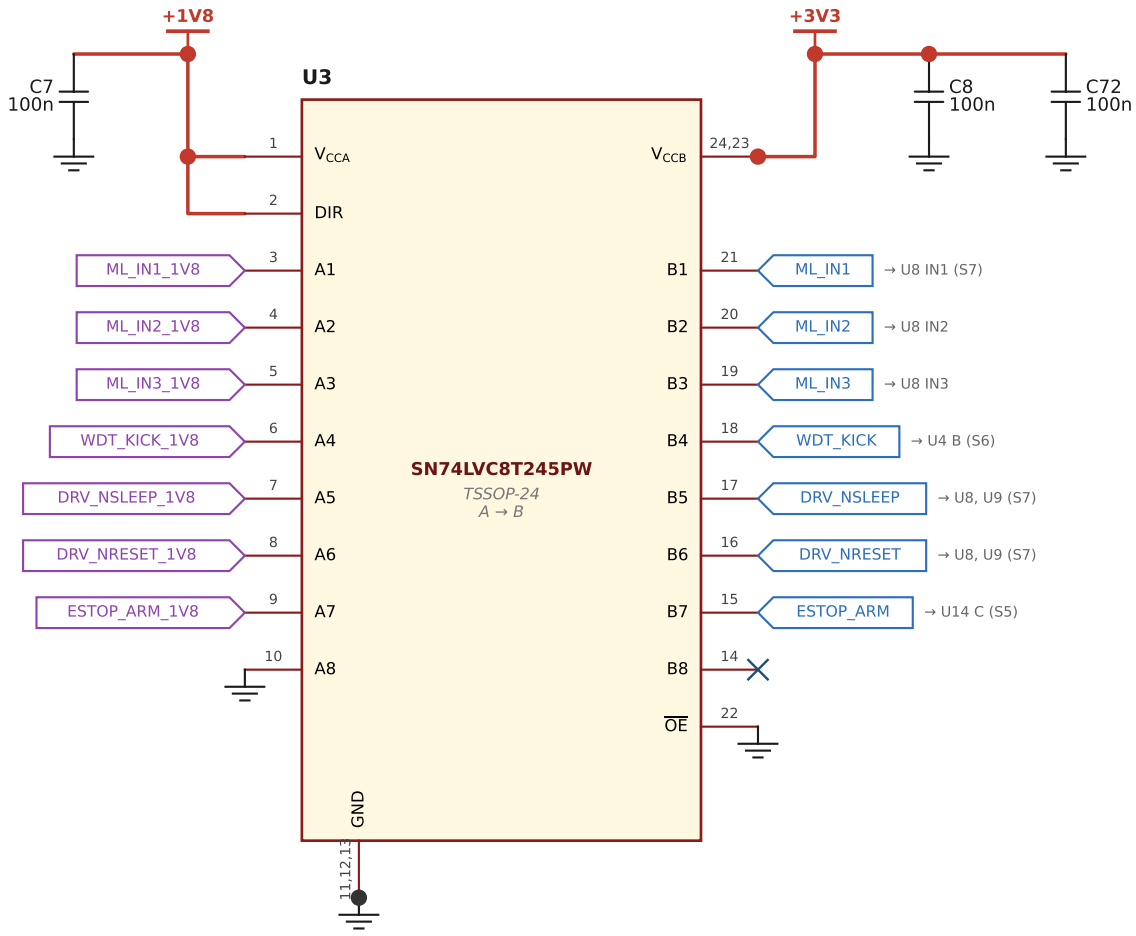
Derived values

- Stall current: 16.8 V / 11.1 Ω ≈ 1.5 A per winding, inside the 2.5 A peak and below the 3 A overcurrent latch.
- Phase copper: 1.0 mm F.Cu carries ≈3.2 A (IPC-2221, 20 °C rise); the 0.35 mm escape from the 0.65 mm-pitch pins carries ≈1.5 A, the firmware's 1.5 A clamp.
- nFAULT pull-up: 3.3 V / 10k = 0.33 mA; D8 lights through 1k while either driver pulls nFAULT low.
- VM range 8–60 V against 12–16.8 V (4S); regen current returns to VBUS through Q2.

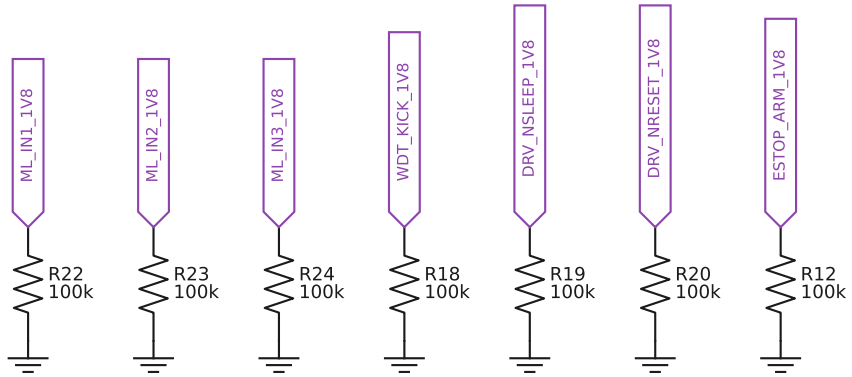
Project	Balance carrier v2 (Milk-V Duo S carrier)
Sheet	**S7 Wheel drivers: 2 × DRV8313 three-phase …**
Revision	v0.9
Source	hardware/kicad/balance_carrier (netlist + symbols)
Generated by	tools/hardware/build_circuits.py
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S8 1.8 V → 3.3 V level translation (U3)

Duo S header J4 is 1.8 V logic. A direction-fixed SN74LVC8T245 lifts the left-wheel PWM, the watchdog kick, the driver sleep/reset lines and the E-stop re-arm to 3.3 V push-pull outputs.



1.8 V-side pull-downs (inputs low while the Duo S boots)



Inputs come from Duo S header J4 (1.8 V): J4-40/42/44 PWM8–10, J4-46 kick, J4-39 sleep, J4-41 reset, J4-36 re-arm (S12). B8 is unused; A8 is tied low.

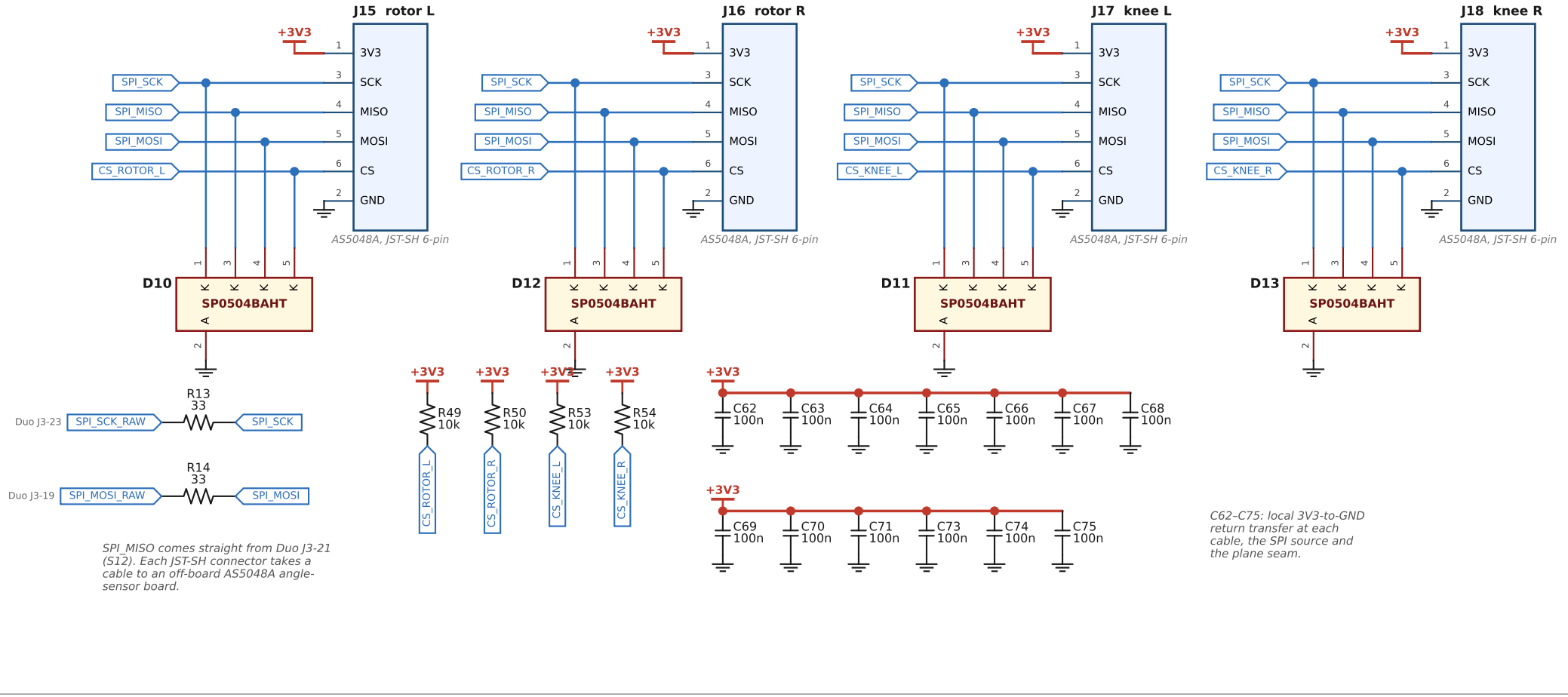
Derived values

- VOH ≥ 2.4 V at 3.3 V VCCB covers the DRV8313's 2.2 V VIH. The push-pull outputs still require return-path, loading and edge-rate validation.
- The 100k pull-downs keep every input low while the Duo S boots; the outputs follow, so the drivers sleep and the watchdog sees no kick.

Project	Balance carrier v2 (Milk-V Duo S carrier)
Sheet	**S8 1.8 V → 3.3 V level translation (U3)**
Revision	v0.9
Source	hardware/kicad/balance_carrier (netlist + symbols)
Generated by	tools/hardware/build_circuits.py
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S9 Angle sensors: SPI3 to 4 × AS5048A

One SPI bus with four chip selects reads both wheel-rotor encoders (FOC and odometry) and both knee encoders. Each sensor is an off-board AS5048A board on a 6-pin JST-SH cable.



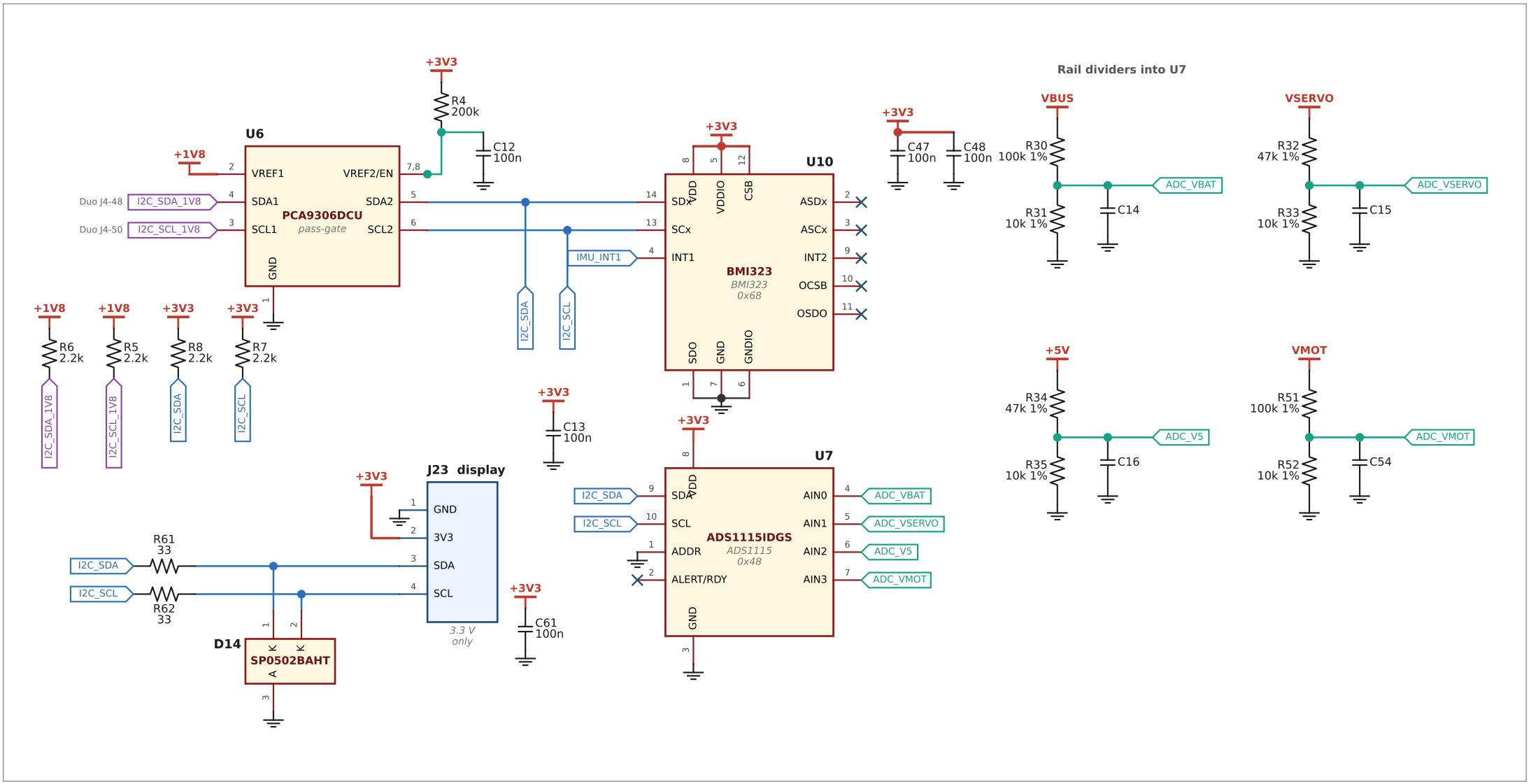
Derived values

- AS5048A: SPI mode 1, 16-bit frames, ≤ 10 MHz; the firmware runs 2–4 MHz over the cables.
- SCK/MOSI source resistors are 33 Ω starting values; tune with the real four-cable load. MISO has one active sensor driver at a time.
- CS pull-ups 10k keep every sensor deselected while the Duo S boots.
- Each 6-pin connector carries 3V3 and GND with the bus, so every cable has its own return.

Project	Balance carrier v2 (Milk-V Duo S carrier)
Sheet	**S9 Angle sensors: SPI3 to 4 × AS5048A**
Revision	v0.9
Source	hardware/kicad/balance_carrier (netlist + symbols)
Generated by	tools/hardware/build_circuits.py
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S10 I2C4: IMU (BMI323) and rail monitor (ADS1115)

Duo S I2C4 is on the 1.8 V header. A PCA9306 passes it to a 3.3 V segment with the on-board BMI323 IMU (balance loop), ADS1115 rail monitor and optional 3.3 V display connector J23.



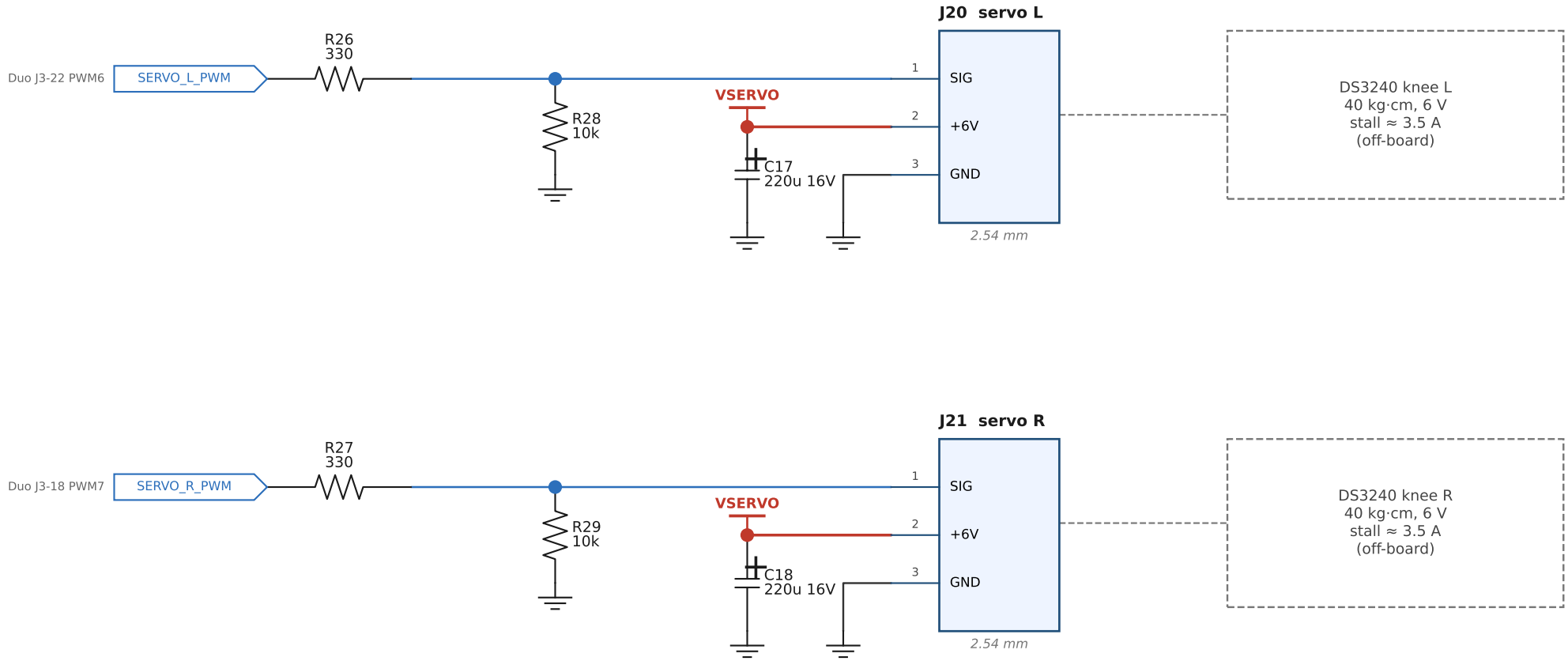
Derived values

- Divider outputs at nominal: VBUS 1.53 V, VSERVO 1.05 V, +5V 0.93 V, VMOT 1.53 V; ADS1115 at ±2.048 V reads up to VBUS 22.5 V, VSERVO 11.7 V, +5V 11.7 V, VMOT 22.5 V.
- VBAT filter: (R30 ‖ R31) × C14 → fc ≈ 175 Hz, well above the monitor's sample rate.
- Pull-ups 2.2k: rise time 0.85·R·C ≈ 94 ns at 50 pF, inside fast-mode's 300 ns.

Project	Balance carrier v2 (Milk-V Duo S carrier)
Sheet	**S10 I2C4: IMU (BMI323) and rail monitor …**
Revision	v0.9
Source	hardware/kicad/balance_carrier (netlist + symbols)
Generated by	tools/hardware/build_circuits.py
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S11 Knee servos: 2 × DS3240 on the 6 V rail

Two hobby-servo headers carry VSERVO, GND and a conditioned PWM signal from Duo S PWM6/7 (50–330 Hz). Each header has its own 220 µF bulk capacitor for the servo's current pulses.



PWM6/7 (A18/A19) are also the little core's JTAG TCK/TMS: JTAG is not available with servos fitted.

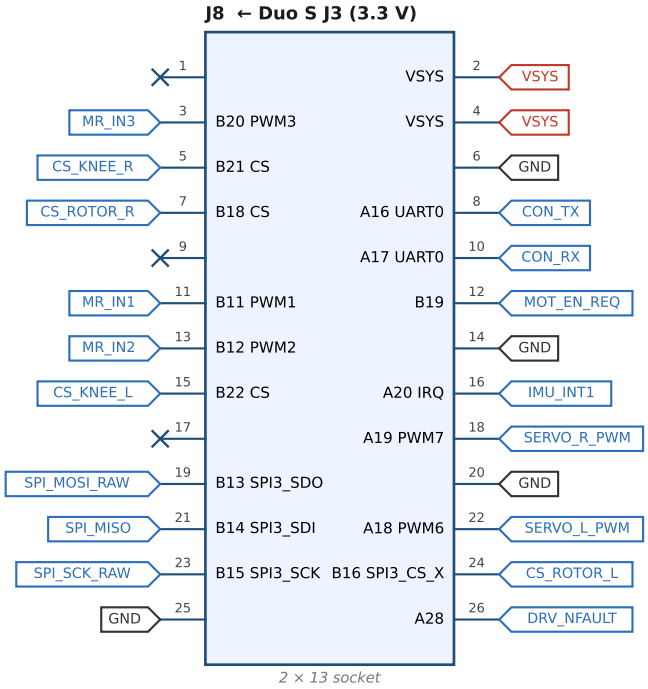
Derived values

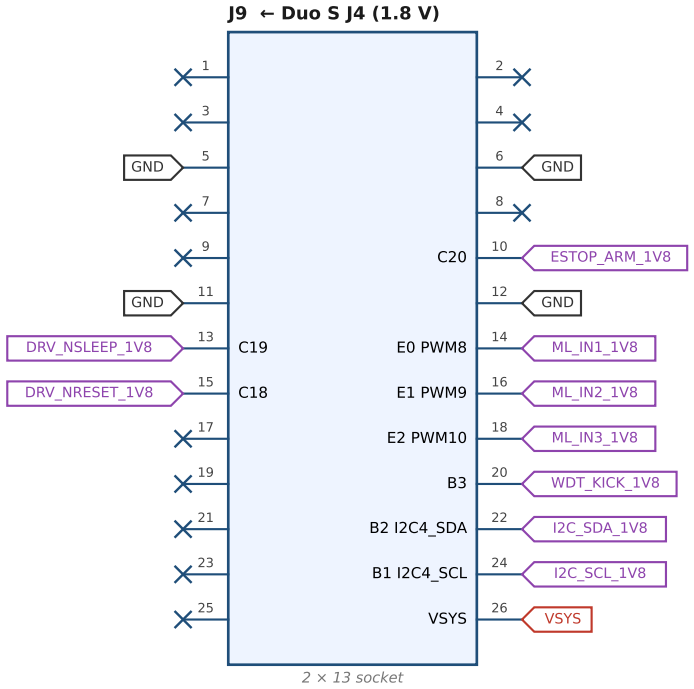
- Series 330 Ω: a servo lead shorted to 6 V pushes at most (6 − 3.3) V / 330 Ω ≈ 8 mA into the Duo pin's clamp.
- Pull-down 10k: no pulses, so the servo idles while the Duo S boots.
- Two stalls ≈ 7 A from the 8 A buck; the 220 µF at each header covers the servo's inrush pulses.

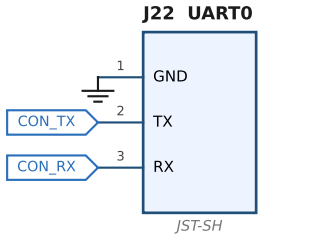
Project	Balance carrier v2 (Milk-V Duo S carrier)
Sheet	**S11 Knee servos: 2 × DS3240 on the 6 V rail**
Revision	v0.9
Source	hardware/kicad/balance_carrier (netlist + symbols)
Generated by	tools/hardware/build_circuits.py
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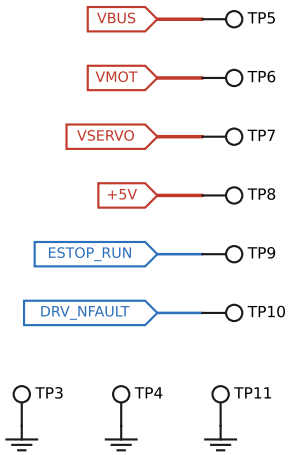
S12 Duo S interface, debug UART and mechanics

The carrier plugs onto a stock Milk-V Duo S with two 2×13 sockets on its bottom side. J8 takes Duo header J3 (3.3 V logic), J9 takes J4 (1.8 V logic). Pins below are coloured by the subsystem that uses them.









Pin names inside J8/J9 are the Duo S functions the carrier uses. X: pad left unconnected (the Duo's own 3V3 pins, J3-9, the audio and MIPI pads).

Mounting: H1/H2 M3 chassis, H5–H8 M2.5 Duo S standoffs



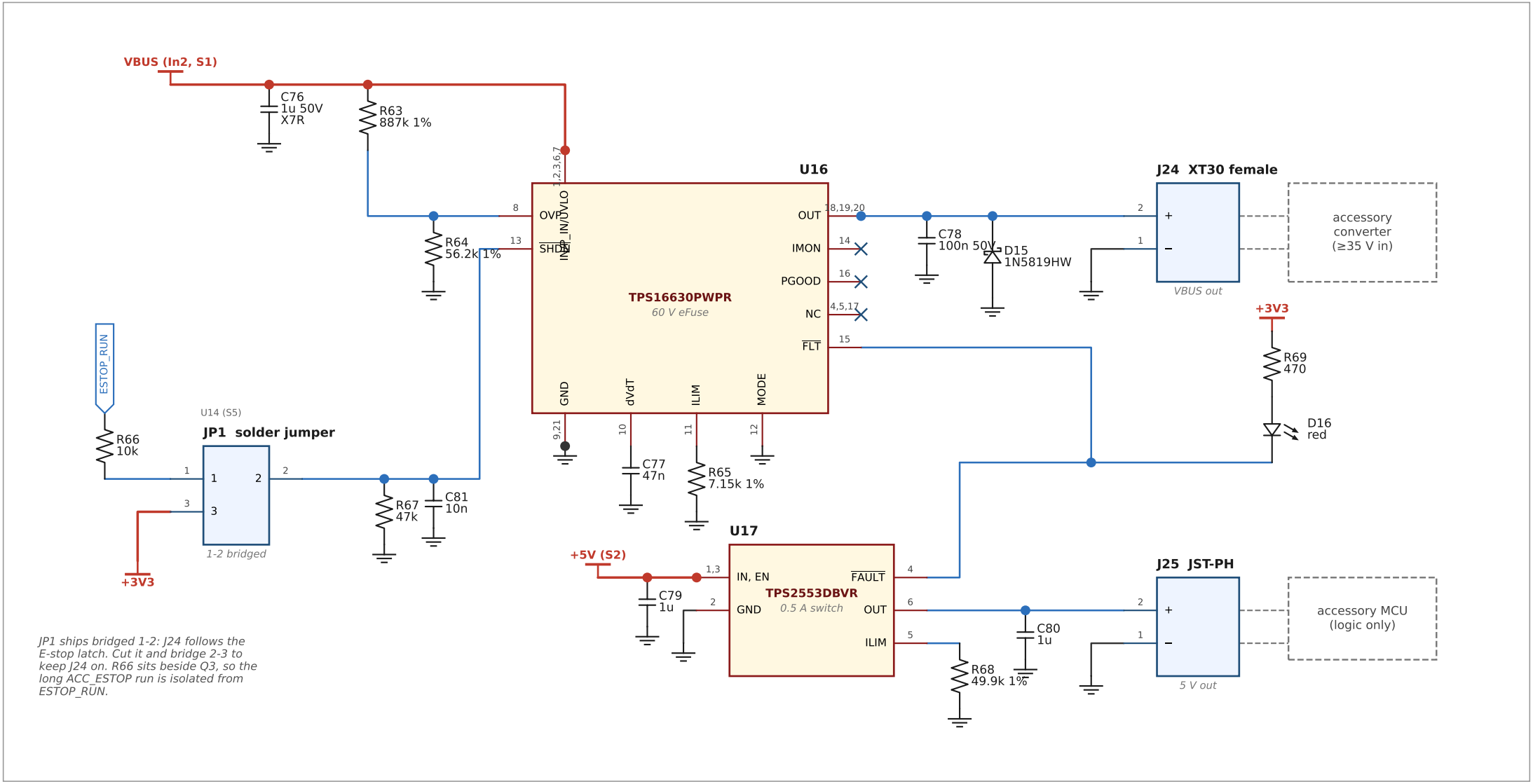
Derived values

- Used pads: J8 19 nets, J9 11 nets (GND and VSYS counted once).
- VSYS reaches the Duo on J3-2, J3-4 and J4-52 from D3 (S4).
- generate_pcb.py fails the build if a socket pad is not exactly on its Duo S pin (Milk-V DUO_S_MB_V1_2-TOP.dxf).

Project	Balance carrier v2 (Milk-V Duo S carrier)
Sheet	**S12 Duo S interface, debug UART and mechanics**
Revision	v0.9
Source	hardware/kicad/balance_carrier (netlist + symbols)
Generated by	tools/hardware/build_circuits.py
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S13 Accessory power outputs: VBUS eFuse (J24) and 5 V switch (J25)

Two outputs for devices off the carrier, such as an accessory MCU and an arm. J24 gives the protected battery voltage through a current-limited eFuse that follows the E-stop by default; J25 gives the 5 V logic rail through a current-limited switch that blocks back-feed.



Derived values

- I(OL) = 18 / R65[kΩ] = 2.52 A (±7 %), fast trip at 2 × I(OL); after about 162 ms in current limit the eFuse turns off and auto-retries.
- OVP = 1.2 V × (R63 + R64)/R64 = 20.1 V, between the 16.8 V full pack and the 32 V TVS clamp.
- Output slew = 1/(20.8 kΩ × C77) = 1.02 V/ms: about 0.48 A into 470 µF, 16.8 V reached in 16 ms.
- SHDN driven high: 3.3 V × R67/(R66 + R67) = 2.72 V (on above 2 V). With U14 unpowered, the pin's 10 µA lifts ESTOP_RUN to at most 0.30 V, below Q3's threshold.
- U17 limit: 23950 / R68[kΩ]^0.977 = 525 mA typical (475–565 mA).
- Fault LED: (3.3 − 2.0) V / 470 Ω ≈ 2.8 mA.

Project	Balance carrier v2 (Milk-V Duo S carrier)
Sheet	**S13 Accessory power outputs: VBUS eFuse (J24) …**
Revision	v0.9
Source	hardware/kicad/balance_carrier (netlist + symbols)
Generated by	tools/hardware/build_circuits.py
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Net index

Every net in the netlist and the sheets it is drawn on. A net on more than one sheet is joined there by its net label or power symbol.

+1V8	S4, S8, S10	BK5_SW	S2	ESTOP_OK	S5	ML_OUT1	S7	U8_CPL	S7
+3V3	S4–S10, S13	BK6_BOOT	S3	ESTOP_RUN	S5–S6, S12–S13	ML_OUT2	S7	U8_V3P3	S7
+5V	S2, S4, S10, S12–S13	BK6_EN	S3	ESTOP_SUPPLY	S5	ML_OUT3	S7	U8_VCP	S7
ACC5_ILIM	S13	BK6_FB	S3	GND	S1–S13	MOT_EN	S6–S7	U9_CPH	S7
ACC_DVDT	S13	BK6_FF	S3	I2C_SCL	S10	MOT_EN_REQ	S5–S6, S12	U9_CPL	S7
ACC_ESTOP	S13	BK6_RT	S3	I2C_SCL_1V8	S10, S12	MR_IN1	S7, S12	U9_V3P3	S7
ACC_ILIM	S13	BK6_SW	S3	I2C_SCL_EXT	S10	MR_IN2	S7, S12	U9_VCP	S7
ACC_NFLT	S13	BK6_VCC	S3	I2C_SDA	S10	MR_IN3	S7, S12	V5_EXT	S13
ACC_OVP	S13	CON_RX	S12	I2C_SDA_1V8	S10, S12	MR_OUT1	S7	VBUS	S1–S3, S5, S10, S12–S1
ACC_SHDN	S13	CON_TX	S12	I2C_SDA_EXT	S10	MR_OUT2	S7	VBUS_EXT	S13
ADC_V5	S10	CS_KNEE_L	S9, S12	I2C_VREF2	S10	MR_OUT3	S7	VMOT	S5, S7, S10, S12
ADC_VBAT	S10	CS_KNEE_R	S9, S12	IMU_INT1	S10, S12	Q1_GATE	S1	VM_DRIVE	S5
ADC_VMOT	S10	CS_ROTOR_L	S9, S12	LED_ACC	S13	SERVO_L_PWM	S11–S12	VM_GATE	S5
ADC_VSERVO	S10	CS_ROTOR_R	S9, S12	LED_EN	S6	SERVO_L_SIG	S11	VSERVO	S3, S10–S12
BAT_FUSED	S1	DRV_NFAULT	S7, S12	LED_FAULT	S7	SERVO_R_PWM	S11–S12	VSYS	S4, S12
BAT_IN	S1	DRV_NRESET	S7–S8	LED_PWR	S4	SERVO_R_SIG	S11	WDT_CEXT	S6
BK5_BOOT	S2	DRV_NRESET_1V8	S8, S12	ML_IN1	S7–S8	SPI_MISO	S9, S12	WDT_KICK	S6, S8
BK5_COMP	S2	DRV_NSLEEP	S7–S8	ML_IN1_1V8	S8, S12	SPI_MOSI	S9	WDT_KICK_1V8	S8, S12
BK5_COMPC	S2	DRV_NSLEEP_1V8	S8, S12	ML_IN2	S7–S8	SPI_MOSI_RAW	S9, S12	WDT_OK	S6
BK5_EN	S2	ESTOP_ARM	S5, S8	ML_IN2_1V8	S8, S12	SPI_SCK	S9	WDT_RCEXT	S6
BK5_FB	S2	ESTOP_ARM_1V8	S8, S12	ML_IN3	S7–S8	SPI_SCK_RAW	S9, S12		
BK5_RT	S2	ESTOP_CLEAR	S5	ML_IN3_1V8	S8, S12	U8_CPH	S7		

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