Balance carrier v2 · v0.9

Subsystem diagrams

Board 100 × 66 mm, 4 layers (F.Cu signal + GND pour, In1.Cu GND plane, In2.Cu logic 3V3 + VBUS, VMOT, VSERVO + lower GND strip + control routing, B.Cu signal + GND pour), 1 oz outer / 1 oz inner, ENIG.

219 footprints, 3517 tracks and vias; unrouted 0, DRC errors 0, schematic-parity issues 0.

Every wire in these diagrams is checked against the netlist, and every part on the board appears on a page.

Values are the board's own; derived values are computed from them; layout checks are measured on the routed copper.

Contents and layout-check summary

page	subsystem	OK	CHECK	FIX
1	Cover			
2	System overview			
3	Board map			
4	S1 Power entry and reverse-polarity protection	1	2	·
5	S2 5 V logic rail: TPS54560B buck (U11)	6	·	·
6	S3 6 V servo rail: LM61480 synchronous buck (U12)	6	2	·
7	S4 Logic rails: VSYS feed, 3.3 V and 1.8 V LDOs	4	·	·
8	S5 E-stop latch and motor-supply switch	3	1	·
9	S6 Motor-enable safety chain: watchdog and AND gate	1	3	·
10	S7 Wheel drivers: 2 × DRV8313 three-phase bridges	4	4	·
11	S8 1.8 V → 3.3 V level translation (U3)	2	3	·
12	S9 Angle sensors: SPI3 to 4 × AS5048A	2	6	·
13	S10 I2C4: IMU (BMI323) and rail monitor (ADS1115)	3	3	·
14	S11 Knee servos: 2 × DS3240 on the 6 V rail	1	2	·
15	S12 Duo S interface, debug UART and mechanics	·	2	·
16	S13 Accessory power outputs: VBUS eFuse (J24) and 5 V switch (J25)	5	2	·

How to read the diagrams

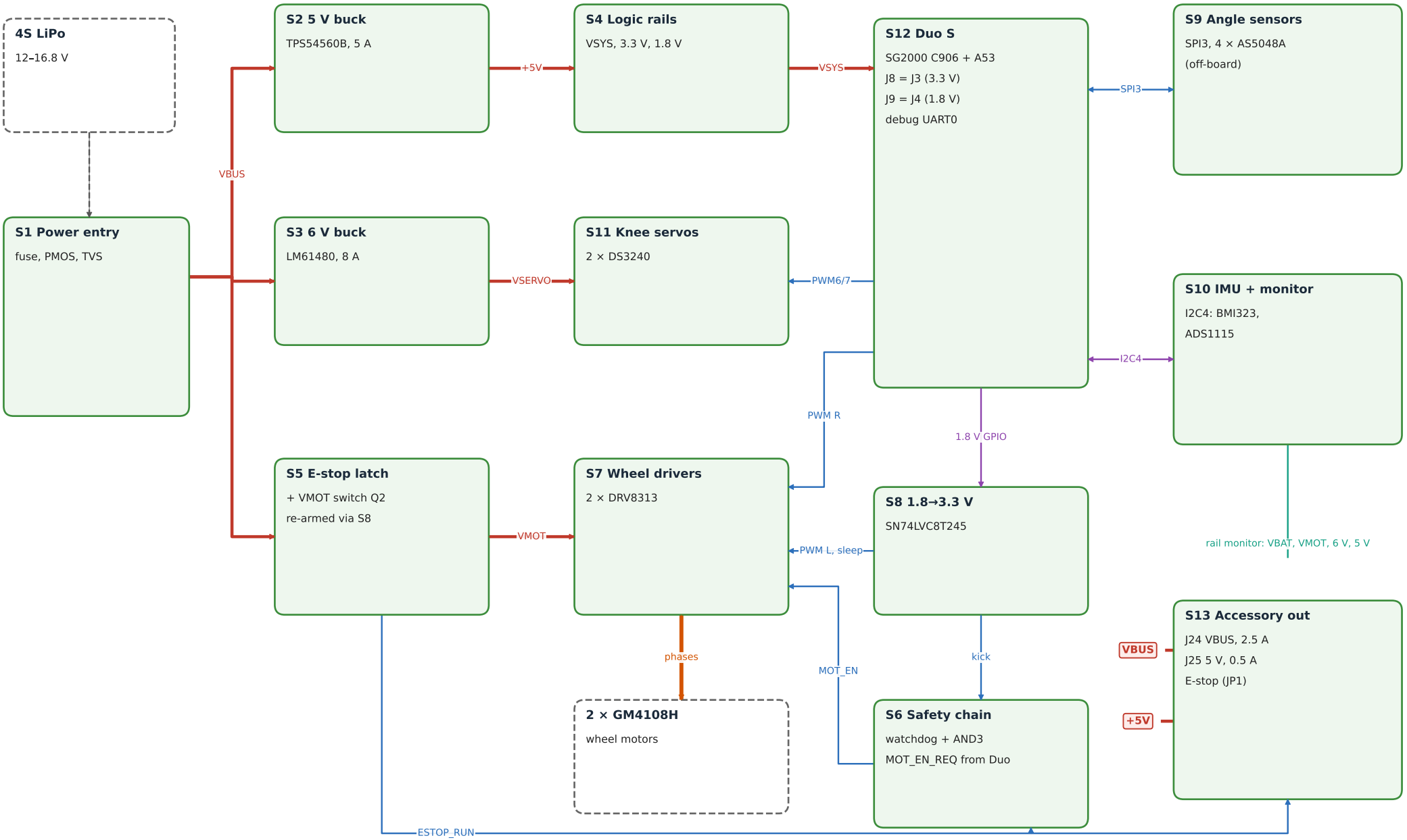
- power rail
- switch node / motor phase
- 3.3 V logic
- 1.8 V logic
- analog / sensitive node
- off-board cable
- IC
- passives
- connector on this board
- part of another subsystem
- rail
- off-board item

- **OK** meets the stated target
- **CHECK** requires review or bench validation
- **FIX** fix in the next layout revision

Plane check: F.Cu references In1 GND. B.Cu references In2, with 3V3 under the logic/encoder area and split power regions on the right. Selected control routes also interrupt In2. Inspect reference continuity. Decoupling distances are geometric; review the complete routed supply/ground loops.

System overview

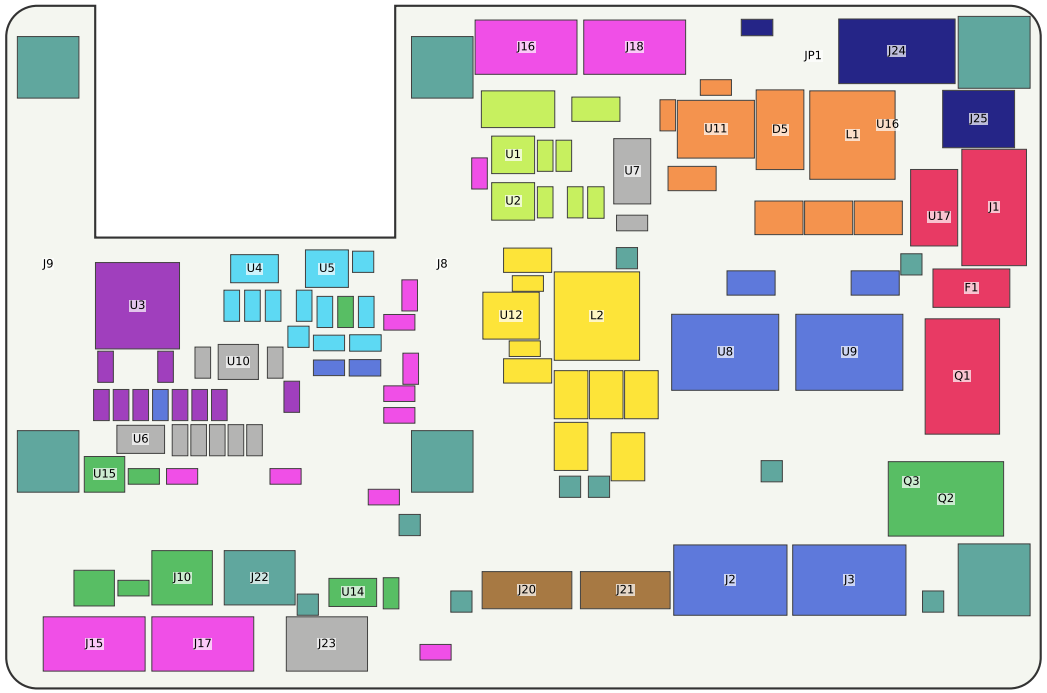
How the thirteen subsystems connect. Red: power rails; blue: 3.3 V logic; purple: 1.8 V logic; orange: motor phases. Each box is one page of this document.



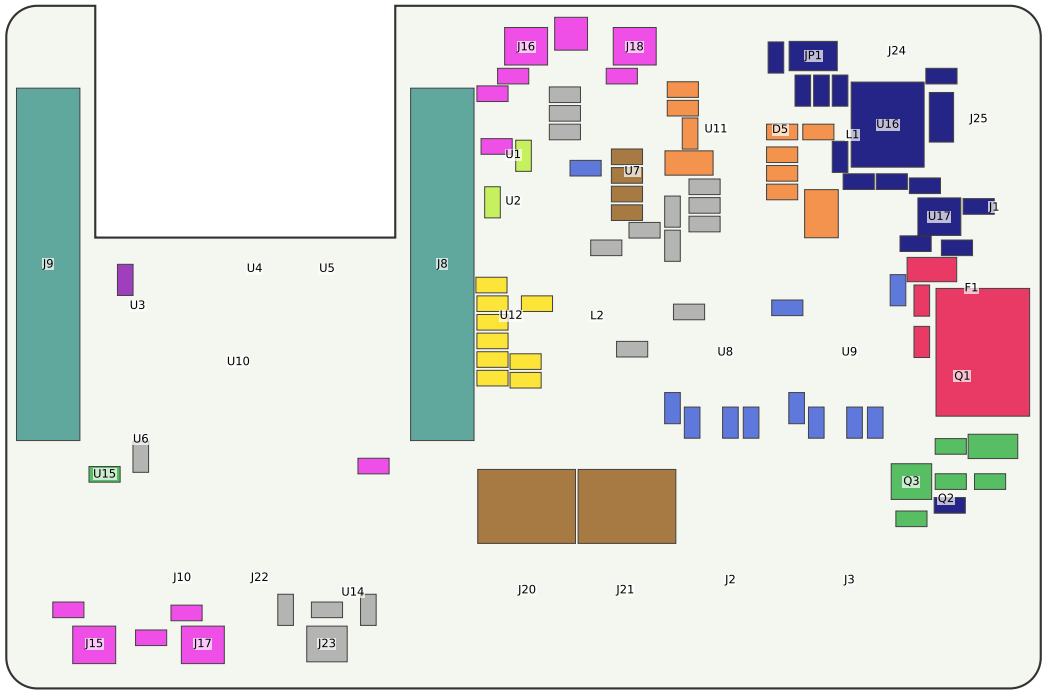
Board map: where each subsystem sits

Footprint outlines from balance_carrier.kicad_pcb, seen from the top. Left: parts on the top side. Right: parts on the bottom side, seen through the board.

Top side



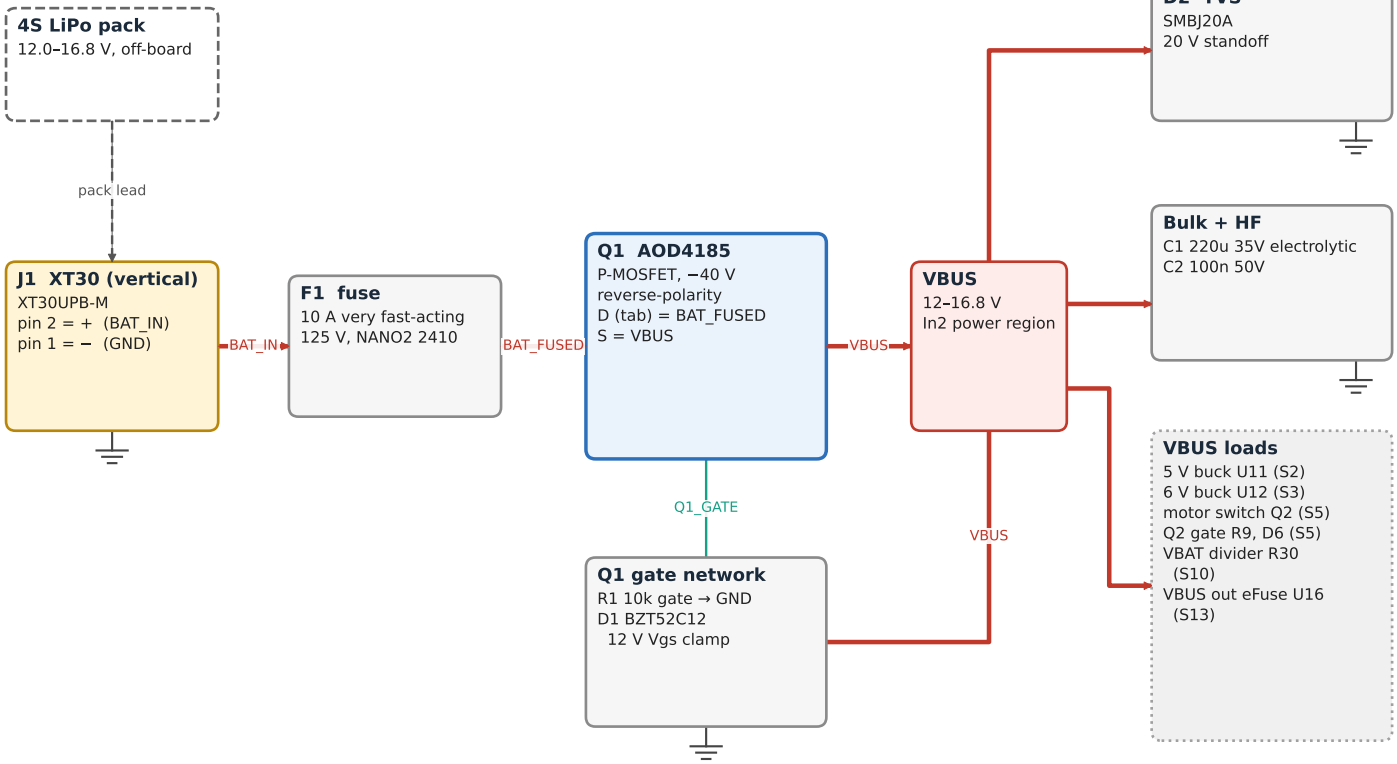
Bottom side (seen through the board)



- S1 Power entry and reverse-polarity protection
- S2 5 V logic rail
- S3 6 V servo rail
- S4 Logic rails
- S5 E-stop latch and motor-supply switch
- S6 Motor-enable safety chain
- S7 Wheel drivers
- S8 1.8 V → 3.3 V level translation (U3)
- S9 Angle sensors
- S10 I2C4
- S11 Knee servos
- S12 Duo S interface, debug UART and mechanics
- S13 Accessory power outputs

S1 Power entry and reverse-polarity protection

Brings the 4S pack in through the XT30, fuses it, blocks a reversed battery with a P-MOSFET and clamps transients. Its output, VBUS, feeds both bucks, the motor-supply switch and the battery monitor.



Where it is (top view; hatched = bottom side)



Layout check (measured on the routed board)

- CHECK — XT30 → fuse (BAT_IN): narrowest 4 mm over 5.3 mm carries ≈8.9 A (IPC-2221, 1 oz outer, 20 °C rise); needs 9.9 A
- CHECK — fuse → Q1 drain tab (BAT_FUSED): narrowest 4 mm over 4.7 mm carries ≈8.9 A (IPC-2221, 1 oz outer, 20 °C rise); needs 9.9 A
- OK — Track segments lying wholly inside a same-net pad (such as the stub Freerouting adds from the 3 mm trace's end, inside Q1's drain tab, to the pad centre) are no constriction and are not counted.

Derived values

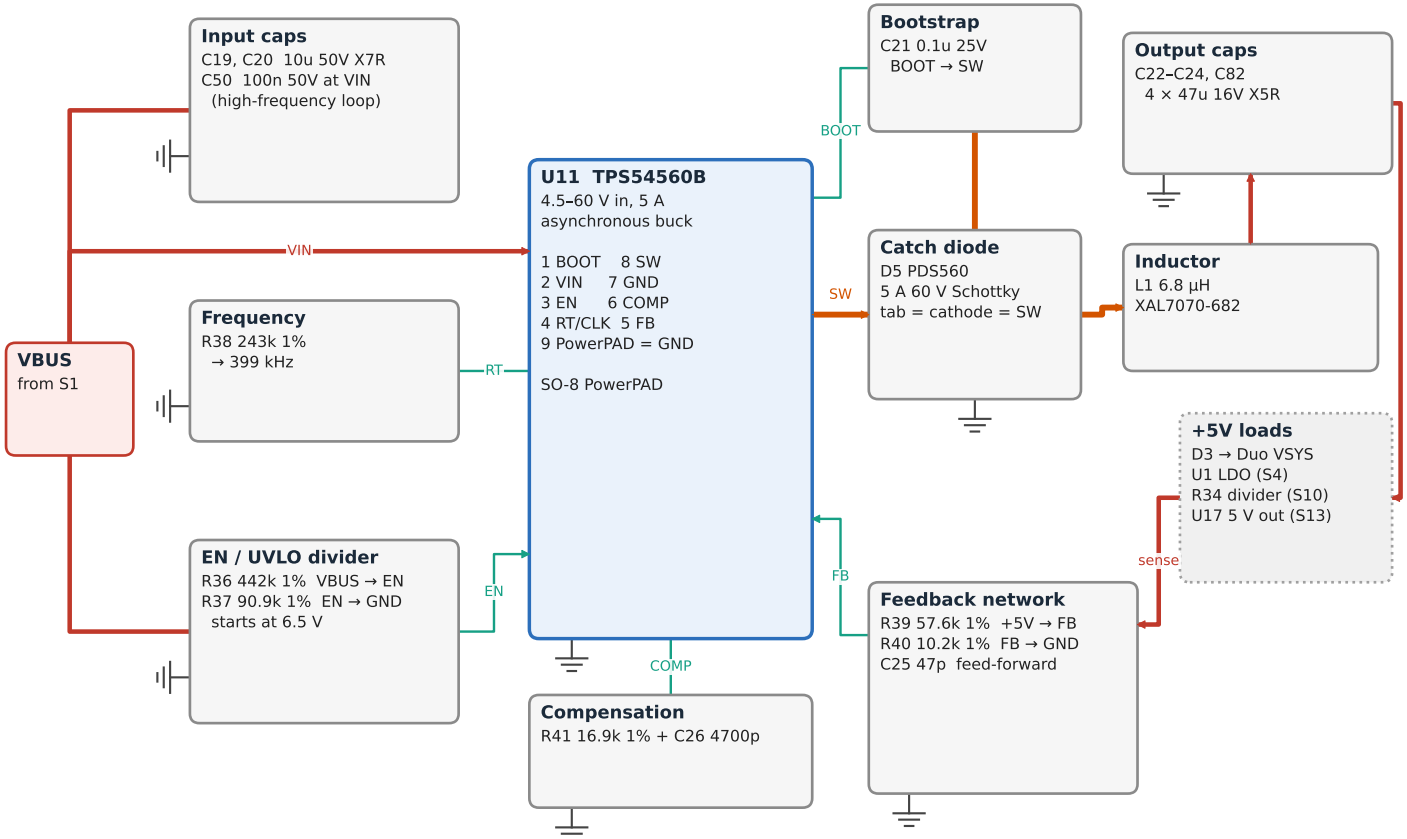
- Q1 gate: R1 holds it at GND, so Vgs = −VBUS: −12 V to −16.8 V. D1 clamps it at −12 V, inside the AOD4185's ±20 V rating.
- Reversed pack: the gate sits at the source and the body diode blocks, so VBUS stays at 0 V.
- D2: 20 V standoff above the 16.8 V full pack, about 32 V clamp; C1 is rated 35 V, every VBUS ceramic 50 V.
- F1: 10 A against about 7.4 A worst case: both motors stalled (3 A), both servos stalled through the 6 V buck on a 12 V pack (4 A), logic (0.4 A). The VBUS accessory output (S13) adds up to its 2.5 A limit: 9.9 A with everything stalled at once, no demonstrated margin.

Notes

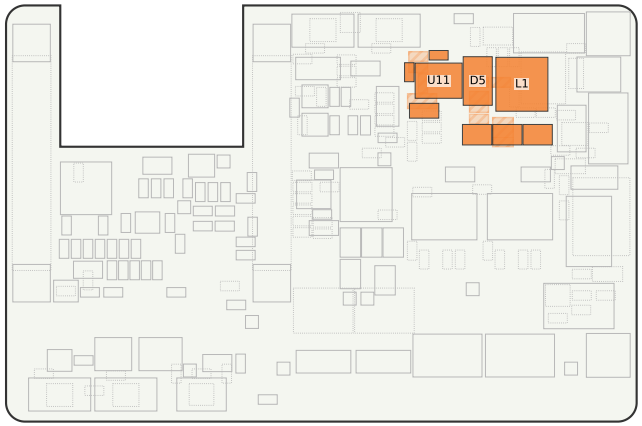
- Measure the battery lead with a meter before first power: XT30 pin 2 must be +.
- Hot-plug: C1 and the buck input caps (about 260 µF) charge through Q1's body diode, so the XT30 sparks. Use an anti-spark lead or a pre-charge resistor.
- Battery current runs on 3.0 mm F.Cu; VBUS spreads through the In2 VBUS region.

S2 5 V logic rail: TPS54560B buck (U11)

Steps VBUS down to 5.32 V for the Duo S (through D3) and the 3.3 V / 1.8 V LDOs. TI's 5 V / 5 A reference design: asynchronous, 400 kHz, external PDS560 catch diode, type-II compensation.



Where it is (top view; hatched = bottom side)



Layout check (measured on the routed board)

- OK — switch node (BK5_SW): 11.6 mm routed, 0 via(s); keep ≤ 12 mm
- OK — bootstrap (BK5_BOOT): 2.9 mm routed, 0 via(s); keep ≤ 5 mm
- OK — feedback node (BK5_FB): 6.7 mm routed, 1 via(s); keep ≤ 8 mm
- OK — RT node (BK5_RT): 5.5 mm routed, 1 via(s); keep ≤ 6 mm
- OK — COMP node (BK5_COMP): 3.1 mm routed, 1 via(s); keep ≤ 6 mm
- OK — U11 pin 2 (VBUS) to nearest GND bypass C50 (100n 50V): 2.1 mm; keep ≤ 3 mm

Derived values

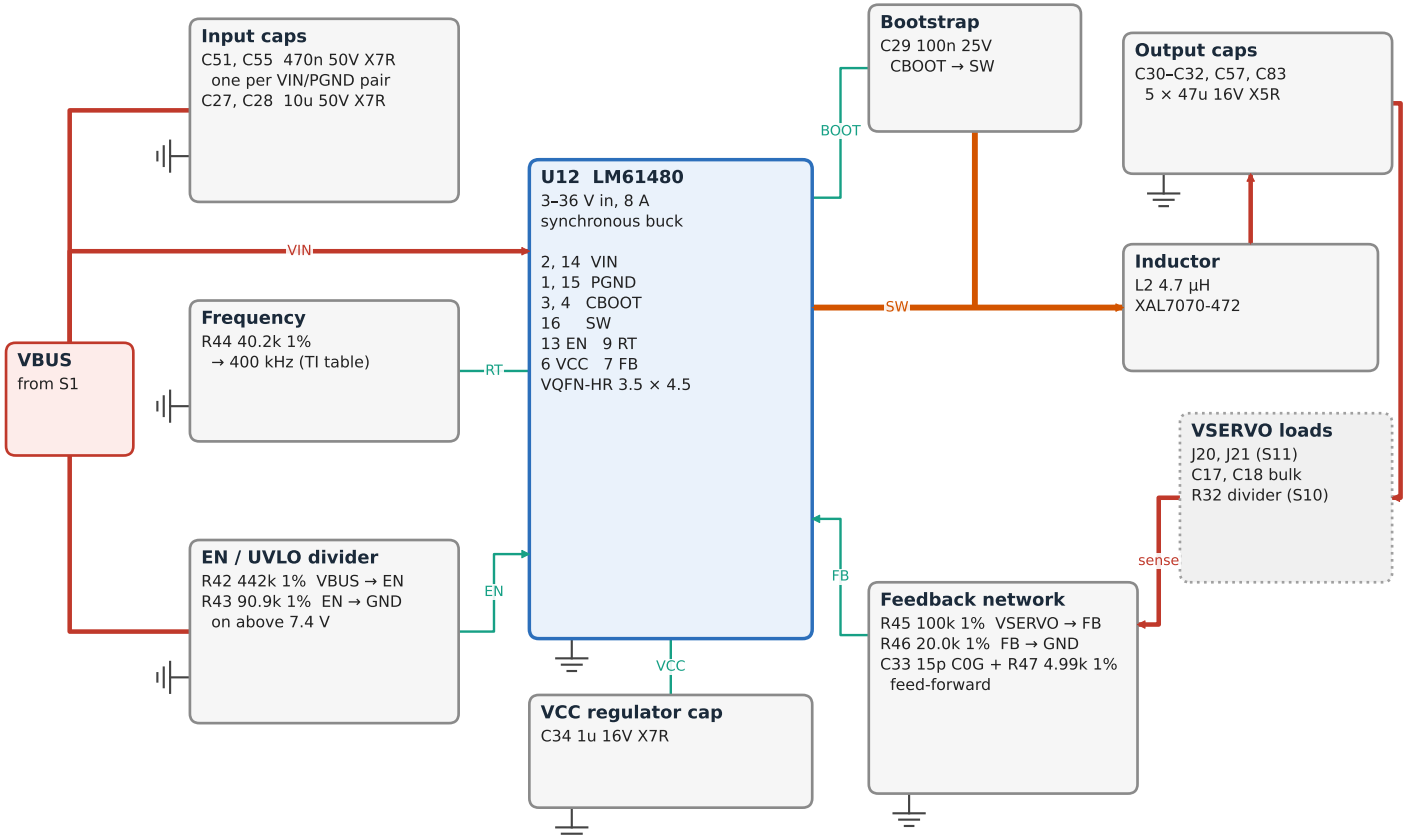
- Vout = 0.8 V × (1 + R39/R40) = 0.8 × (1 + 57.6k/10.2k) = 5.32 V; VSYS is one SS34 drop lower, about 4.9 V.
- fsw = (101756 / RT[kΩ])^(1/1.008) = 399 kHz (TPS54560 datasheet).
- UVLO start = 1.2 V × (1 + R36/R37) − 1.2 µA × R36 = 6.5 V, below a flat 4S pack (12 V).
- Inductor ripple at 16.8 V in: ΔI = (Vin − Vout)·Vout / (Vin·L·f) = 1.34 A p-p (load about 1.2 A, plus up to 0.5 A through the 5 V accessory output; U11 limit 5 A).

Notes

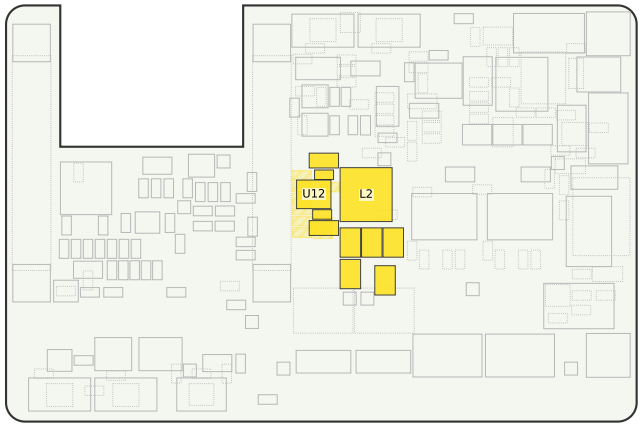
- Hot loop: VIN cap C50 → U11 VIN/GND → D5 → back to C50. Keep it small and on one layer.
- The PowerPAD, D5's anode and the cap grounds pour solidly into GND (no thermal spokes).
- RT, FB and COMP are high-impedance nodes: keep them short and away from SW.

S3 6 V servo rail: LM61480 synchronous buck (U12)

Steps VBUS down to 6.0 V at up to 8 A for the two DS3240 knee servos. Synchronous, 400 kHz, internal compensation with a feed-forward RC, values from TI SNVSBZ4A section 9.2.



Where it is (top view; hatched = bottom side)



Derived values

- Vout = 1.0 V × (1 + R45/R46) = 1.0 × (1 + 100k/20k) = 6.00 V.
- Precision-EN UVLO: on at 1.263 V × (1 + R42/R43) = 7.4 V.
- Inductor ripple at 16.8 V in: ΔI = (Vin − Vout)·Vout / (Vin·L·f) = 2.05 A p-p; XAL7070-472: 15.2 A at 30% L reduction (25°C), versus 13.8 A typical / 15.6 A maximum IC limit; hot/fault margin remains to be verified.
- Two stalled DS3240s draw about 7 A. IC rating is 8 A; usable continuous and burst current require thermal/load measurements on this PCB.

Notes

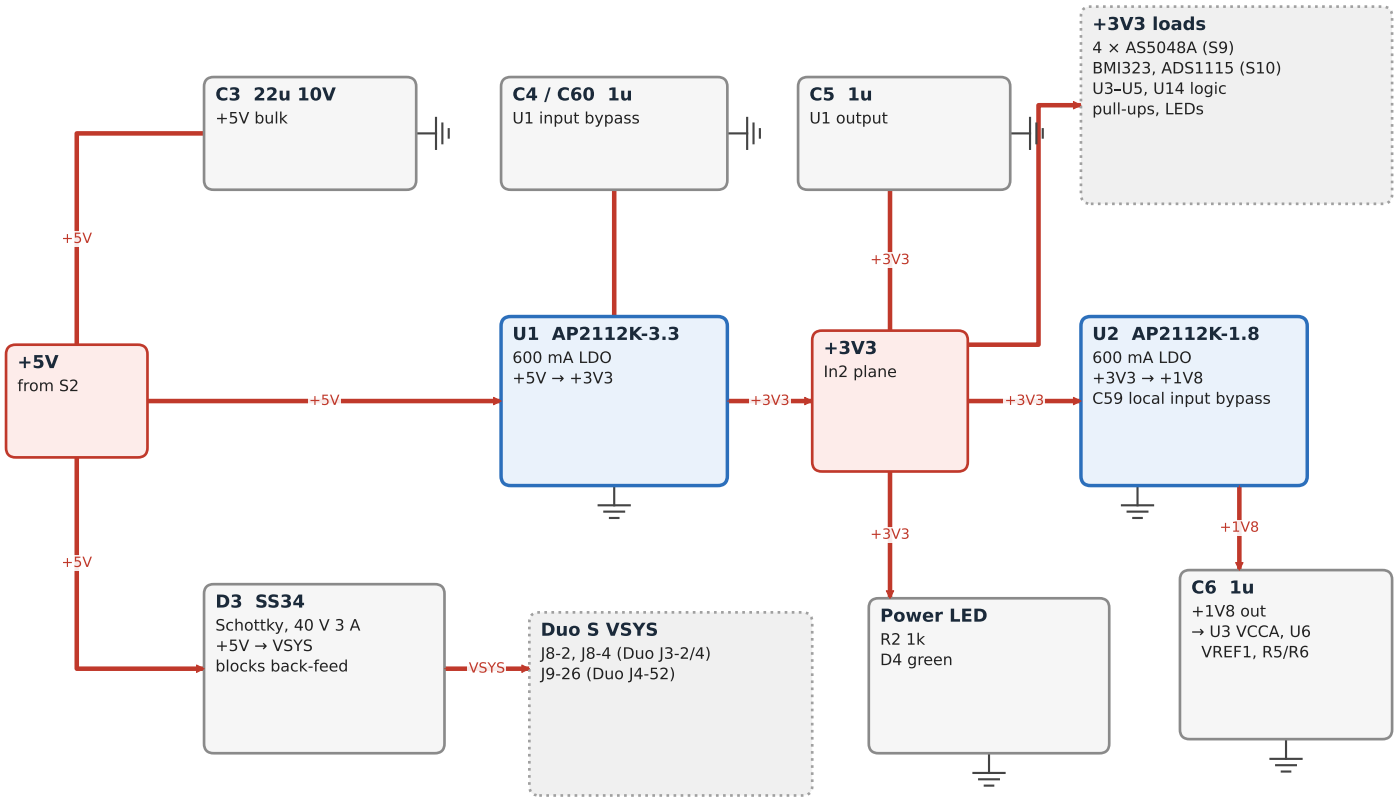
- Each VIN/PGND pin pair has its own 470 nF cap right at the package (the hot loop); the 10 µF caps sit beyond them with VBUS vias into the In2 pocket.
- The SW bar leaves between the PGND corner pads at 1.0 mm and widens to 2.0 mm to L2.
- The FB divider is on the bottom side under the package, fed by a VSERVO sense trace.

Layout check (measured on the routed board)

OK	switch node (BK6_SW): 6.4 mm routed, 1 via(s); keep ≤ 8 mm
OK	bootstrap loop (BK6_BOOT): 5.5 mm routed, 1 via(s); keep ≤ 6 mm
CHECK	feedback node (BK6_FB): 12.7 mm routed, 1 via(s); keep ≤ 10 mm
OK	RT node (BK6_RT): 4.9 mm routed, 1 via(s); keep ≤ 8 mm
OK	VCC cap (BK6_VCC): 3.5 mm routed, 1 via(s); keep ≤ 5 mm
OK	U12 pin 2 (VBUS) to nearest GND bypass C55 (470n 50V X7R): 1.8 mm; keep ≤ 3 mm
OK	U12 pin 14 (VBUS) to nearest GND bypass C51 (470n 50V X7R): 1.7 mm; keep ≤ 3 mm
CHECK	R45 sits 3.1 mm from the FB pin, so the high-impedance FB node is the long run. Put R45 beside R46/R47 and make the low-impedance VSERVO sense the long trace.

S4 Logic rails: VSYS feed, 3.3 V and 1.8 V LDOs

Feeds the Duo S from the 5 V buck through a Schottky (so a USB-C supply on the Duo cannot back-feed the carrier), and makes the 3.3 V logic/sensor rail and the 1.8 V translator reference.



Where it is (top view; hatched = bottom side)



Layout check (measured on the routed board)

- OK — U1 pin 1 (+5V) to nearest GND bypass C60 (1u): 2.1 mm; keep ≤ 3 mm
- OK — U1 pin 5 (+3V3) to nearest GND bypass C5 (1u): 2.0 mm; keep ≤ 3 mm
- OK — U2 pin 1 (+3V3) to nearest GND bypass C59 (1u): 0.9 mm; keep ≤ 3 mm
- OK — U2 pin 5 (+1V8) to nearest GND bypass C6 (1u): 2.0 mm; keep ≤ 3 mm

Derived values

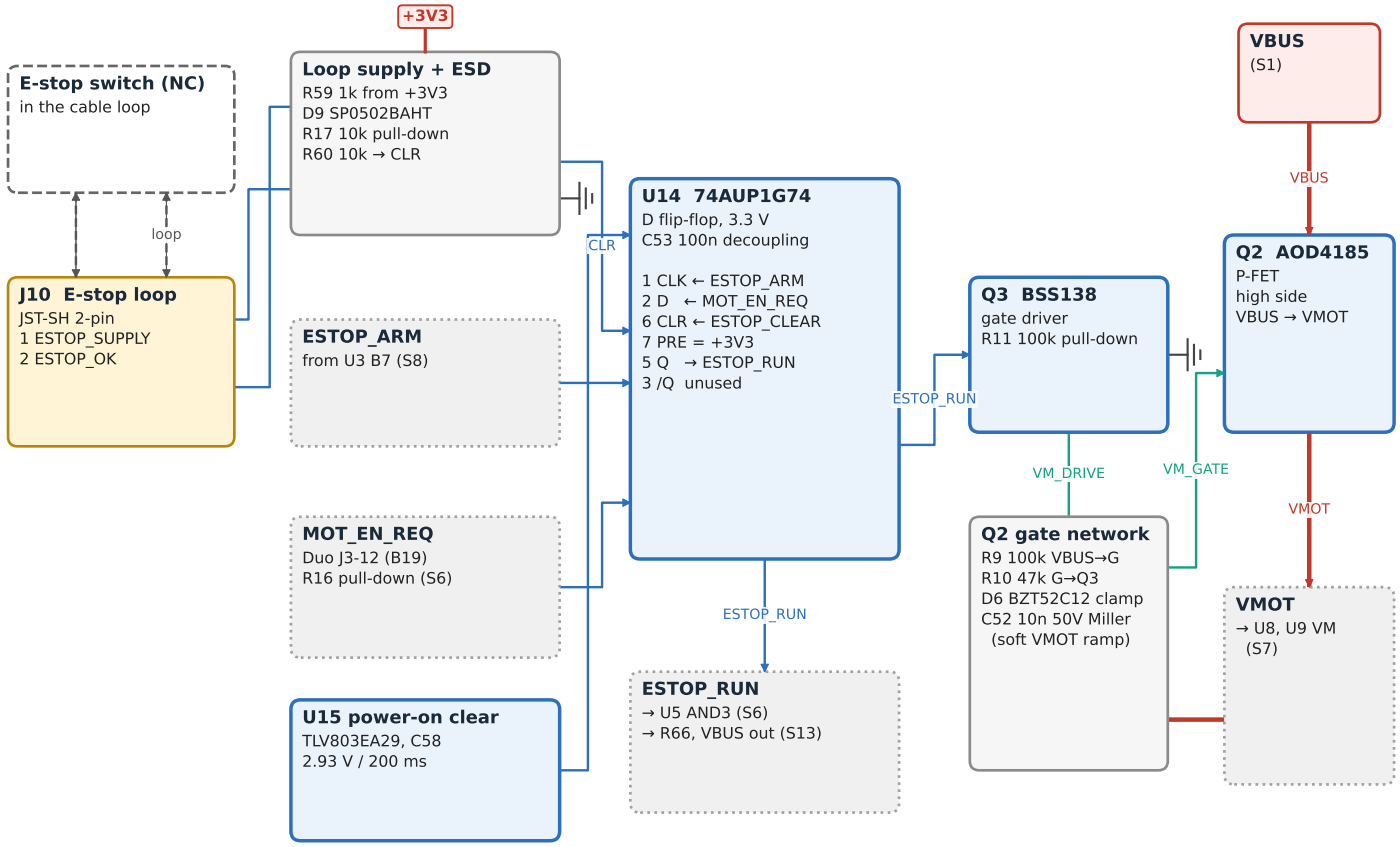
- VSYS ≈ 5.32 V − 0.45 V (SS34 at about 1 A) ≈ 4.9 V at the Duo S.
- U1: (5.32 − 3.3) V × about 90 mA ≈ 0.18 W in a SOT-23-5. U2: (3.3 − 1.8) V × <5 mA, negligible.
- Power LED: (3.3 − 2.0) V / 1k ≈ 1.3 mA.

Notes

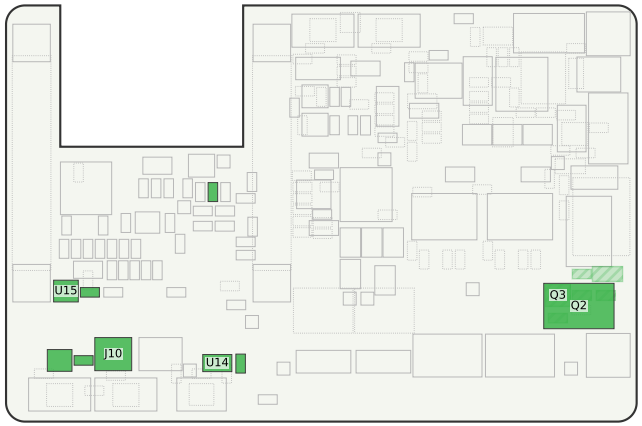
- Do not power the Duo S from USB-C and the carrier together until you have checked how the Duo ties VSYS and USB VBUS: D3 only stops current flowing back into the carrier.
- +3V3 uses the In2 logic region with selected control routes; +1V8 remains routed. Local capacitors transfer SPI returns between the 3V3 reference and GND.

S5 E-stop latch and motor-supply switch

A normally-closed E-stop loop clears a D flip-flop the instant it opens. The latch drives the high-side P-MOSFET that makes VMOT for both motor drivers, so an open loop removes motor power in hardware.



Where it is (top view; hatched = bottom side)



Layout check (measured on the routed board)

- OK — U14 pin 8 (+3V3) to nearest GND bypass C53 (100n): 2.8 mm; keep ≤ 3 mm
- OK — Q2 gate drive (VM_GATE): 16.8 mm routed, 1 via(s); keep ≤ 25 mm
- OK — ESTOP_OK: 0.2 of 58 mm without a plane under it (slow signal)
- CHECK — ESTOP_RUN: 4.9 of 151 mm without a plane under it (slow signal)

Derived values

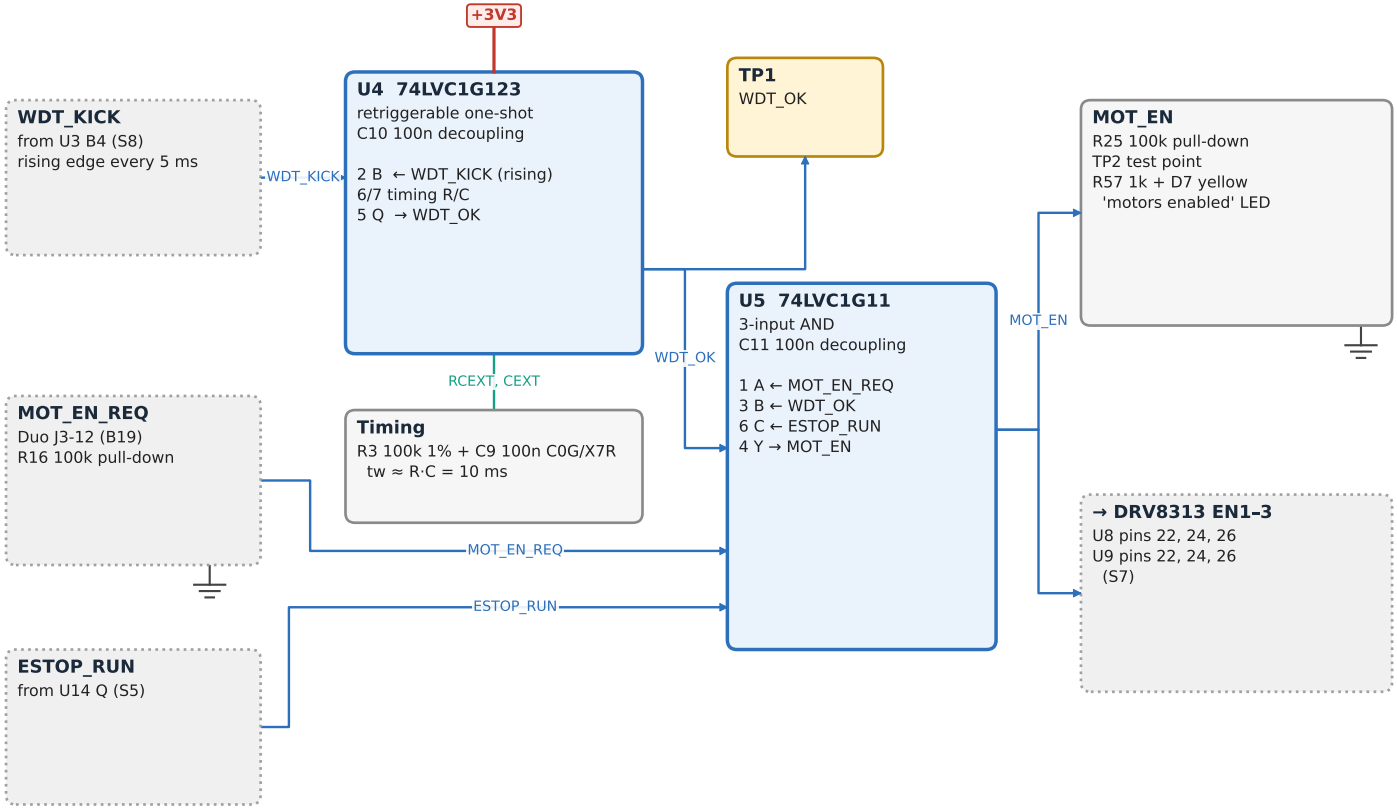
- Q2 on: Vgs = −VBUS × R9/(R9 + R10) = −8.2 V at 12 V, −11.4 V at 16.8 V; D6 clamps at −12 V for transients.
- Loop current 0.30 mA; ESTOP_OK sits at 3.3 V × R17/(R59 + R17) = 3.0 V while closed.
- CLR is asynchronous: opening the loop drops ESTOP_RUN at once, and a bouncing switch cannot set it again.
- C52 makes Q2 a Miller ramp of roughly 30 V/ms, so the DRV8313 bulk caps charge softly; R9 turns it off in about 2 ms; VMOT rail decay is a separate measurement.

Notes

- Re-arm needs all three: loop closed, MOT_EN_REQ high (D), then a rising edge on ESTOP_ARM.
- U15 holds CLR low on startup/brownout, releasing after 130–270 ms above its threshold. A new ARM edge is required; firmware also initializes MOT_EN_REQ low.
- R59 (1 kΩ) means a shorted E-stop cable cannot pull down +3V3.

S6 Motor-enable safety chain: watchdog and AND gate

MOT_EN = MOT_EN_REQ AND WDT_OK AND ESTOP_RUN drives every DRV8313 enable pin. WDT_OK comes from a retriggerable one-shot the control loop must keep kicking, so a hung core disables the bridges within about 10 ms without any software involved.



Where it is (top view; hatched = bottom side)



Layout check (measured on the routed board)

- CHECK — U4 pin 8 (+3V3) to nearest GND bypass C10 (100n): 3.5 mm; keep ≤ 3 mm
- CHECK — U5 pin 5 (+3V3) to nearest GND bypass C11 (100n): 4.3 mm; keep ≤ 3 mm
- CHECK — MOT_EN: 5.7 of 101 mm without a plane under it (slow signal)
- OK — WDT_KICK: 0.6 of 23 mm without a plane under it (slow signal)

Derived values

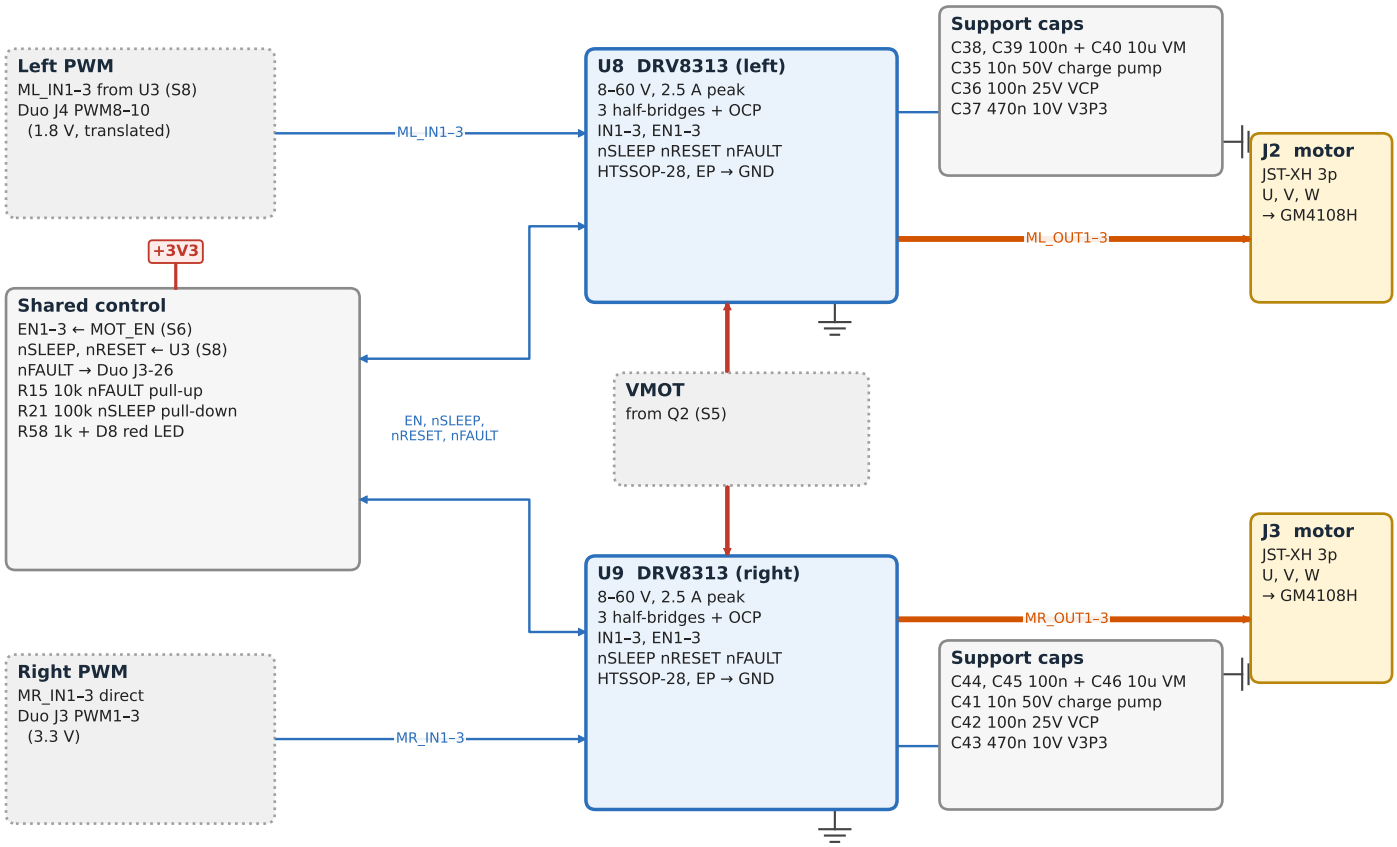
- One-shot width tw ≈ K·R3·C9 with K ≈ 1: 10 ms, twice the 5 ms kick period at 400 Hz.
- Edge-triggered, so a core stuck with WDT_KICK high or low both time out.
- LED D7: (3.3 − 2.0) V / 1k ≈ 1.3 mA from MOT_EN.
- Pull-downs on MOT_EN_REQ and MOT_EN keep the bridges off while the Duo S boots.

Notes

- Measure the real pulse width on TP1: the 74LVC1G123's K factor varies with VCC and C.
- TP2 shows MOT_EN for bring-up (BRINGUP.md stage 5).

S7 Wheel drivers: 2 × DRV8313 three-phase bridges

Each DRV8313 drives one GM4108H gimbal motor with three PWM half-bridges for FOC. VMOT comes from the E-stop switch (S5); the enables come from the safety chain (S6).



Where it is (top view; hatched = bottom side)



Layout check (measured on the routed board)

- CHECK left phase U (ML_OUT1): narrowest 0.35 mm over 3.0 mm carries ≈1.5 A (IPC-2221, 1 oz outer, 20 °C rise); needs 2.5 A
- CHECK right phase U (MR_OUT1): narrowest 0.35 mm over 3.0 mm carries ≈1.5 A (IPC-2221, 1 oz outer, 20 °C rise); needs 2.5 A
- CHECK U8 pin 4 (VMOT) to nearest GND bypass C38 (100n 50V): 5.5 mm; keep ≤ 5 mm
- CHECK U9 pin 4 (VMOT) to nearest GND bypass C44 (100n 50V): 5.5 mm; keep ≤ 5 mm
- OK U8 pin 15 (U8_V3P3) to nearest GND bypass C37 (470n 10V): 1.8 mm; keep ≤ 3 mm
- OK U9 pin 15 (U9_V3P3) to nearest GND bypass C43 (470n 10V): 2.4 mm; keep ≤ 3 mm
- OK U8 charge pump (U8_CPL): 2.4 mm routed, 1 via(s); keep ≤ 6 mm
- OK U9 charge pump (U9_CPL): 2.4 mm routed, 1 via(s); keep ≤ 6 mm

Derived values

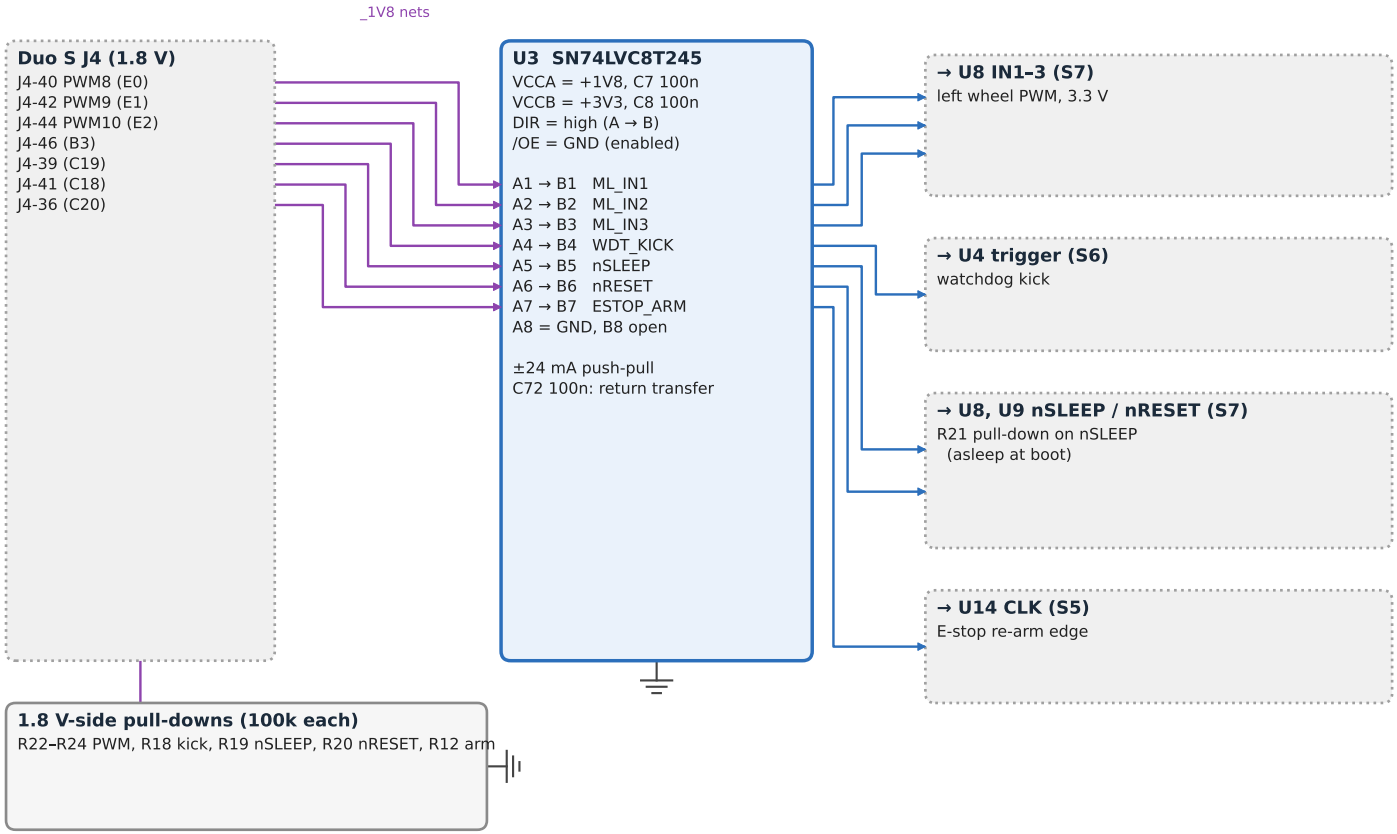
- Stall current: 16.8 V / 11.1 Ω ≈ 1.5 A per winding, inside the 2.5 A peak and below the 3 A overcurrent latch.
- Phase copper: 1.0 mm F.Cu carries ≈3.2 A (IPC-2221, 20 °C rise); the 0.35 mm escape from the 0.65 mm-pitch pins carries ≈1.5 A, the firmware's 1.5 A clamp.
- nFAULT pull-up: 3.3 V / 10k = 0.33 mA; D8 lights through 1k while either driver pulls nFAULT low.
- VM range 8–60 V against 12–16.8 V (4S); regen current returns to VBUS through Q2.

Notes

- U9 (right) takes 3.3 V PWM straight from Duo J3; U8 (left) needs U3 because Duo J4 is 1.8 V, below the DRV8313's 2.2 V VIH.
- Each wheel's three phases are on one SG2000 PWM controller, so the three duties update together.
- Exposed pads: 2 × 4 thermal via array each; order the vias tented or filled.

S8 1.8 V → 3.3 V level translation (U3)

Duo S header J4 is 1.8 V logic. A direction-fixed SN74LVC8T245 lifts the left-wheel PWM, the watchdog kick, the driver sleep/reset lines and the E-stop re-arm to 3.3 V push-pull outputs.



Where it is (top view; hatched = bottom side)



Layout check (measured on the routed board)

●	OK	U3 pin 1 (+1V8) to nearest GND bypass C7 (100n): 1.6 mm; keep ≤ 3 mm
●	OK	U3 pin 24 (+3V3) to nearest GND bypass C8 (100n): 1.6 mm; keep ≤ 3 mm
●	CHECK	ML_IN1: 3.6 of 74 mm without a plane under it (fast edges)
●	CHECK	ML_IN3_1V8: 2.1 of 49 mm without a plane under it (fast edges)
●	CHECK	DRV_NRESET: 6.2 of 94 mm without a plane under it (slow signal)

Derived values

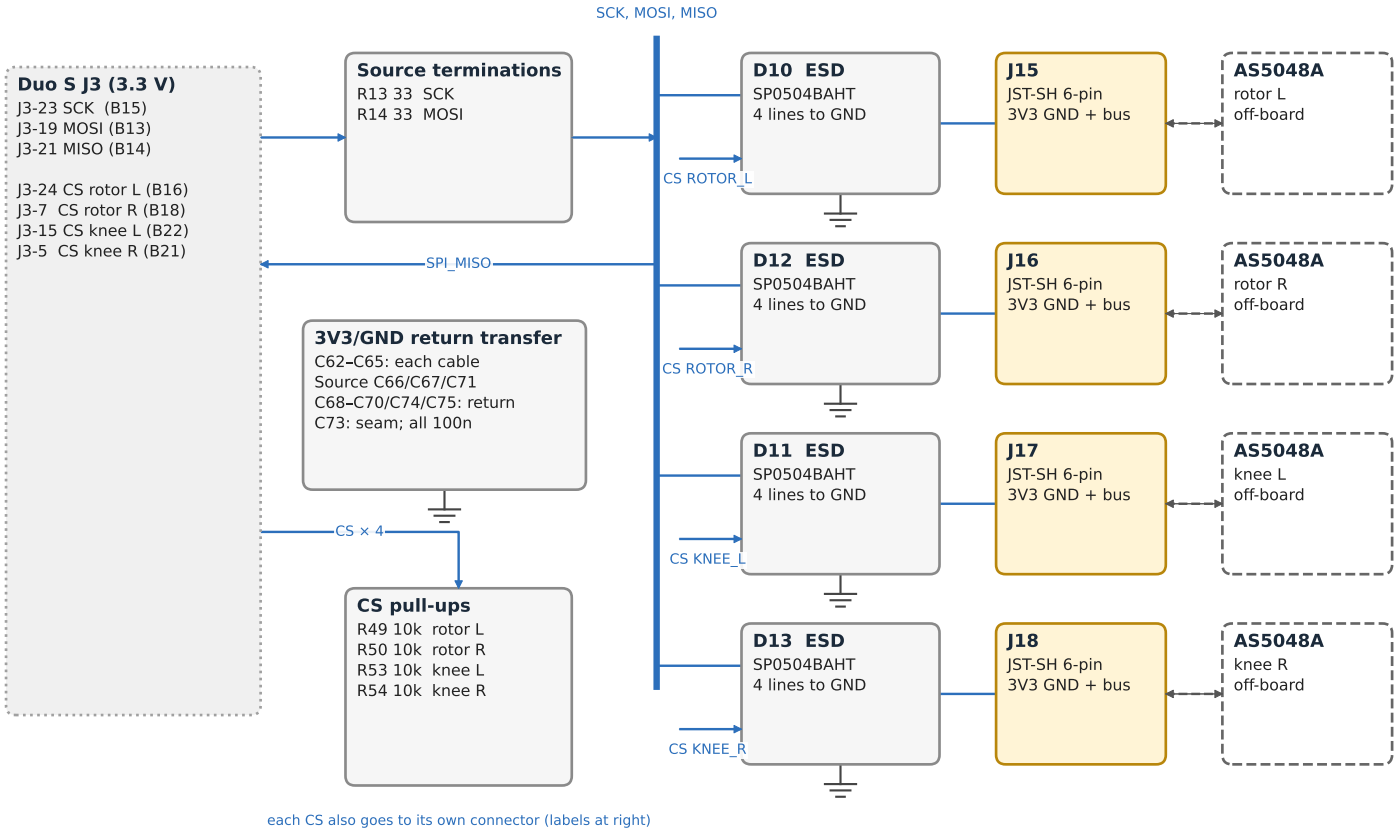
- VOH ≥ 2.4 V at 3.3 V VCCB covers the DRV8313's 2.2 V VIH. The push-pull outputs still require return-path, loading and edge-rate validation.
- The 100k pull-downs keep every input low while the Duo S boots; the outputs follow, so the drivers sleep and the watchdog sees no kick.

Notes

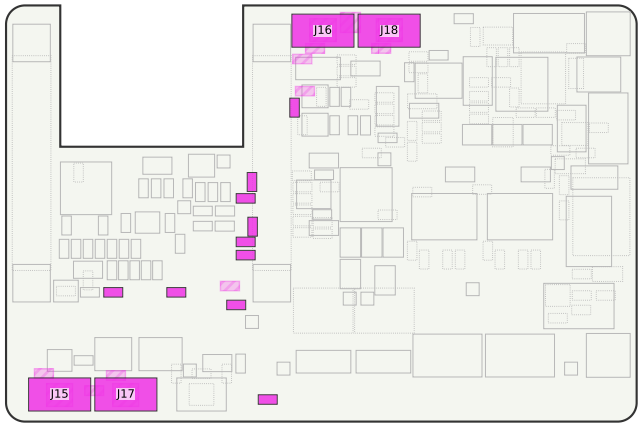
- Duo J4 also carries I2C4, which goes through U6 (PCA9306, S10), not through U3.
- Linux must not claim these pads: the C906 firmware owns the pinmux (see the port README).

S9 Angle sensors: SPI3 to 4 × AS5048A

One SPI bus with four chip selects reads both wheel-rotor encoders (FOC and odometry) and both knee encoders. Each sensor is an off-board AS5048A board on a 6-pin JST-SH cable.



Where it is (top view; hatched = bottom side)



Derived values

- AS5048A: SPI mode 1, 16-bit frames, ≤ 10 MHz; the firmware runs 2–4 MHz over the cables.
- SCK/MOSI source resistors are 33 Ω starting values; tune with the real four-cable load. MISO has one active sensor driver at a time.
- CS pull-ups 10k keep every sensor deselected while the Duo S boots.
- Each 6-pin connector carries 3V3 and GND with the bus, so every cable has its own return.

Notes

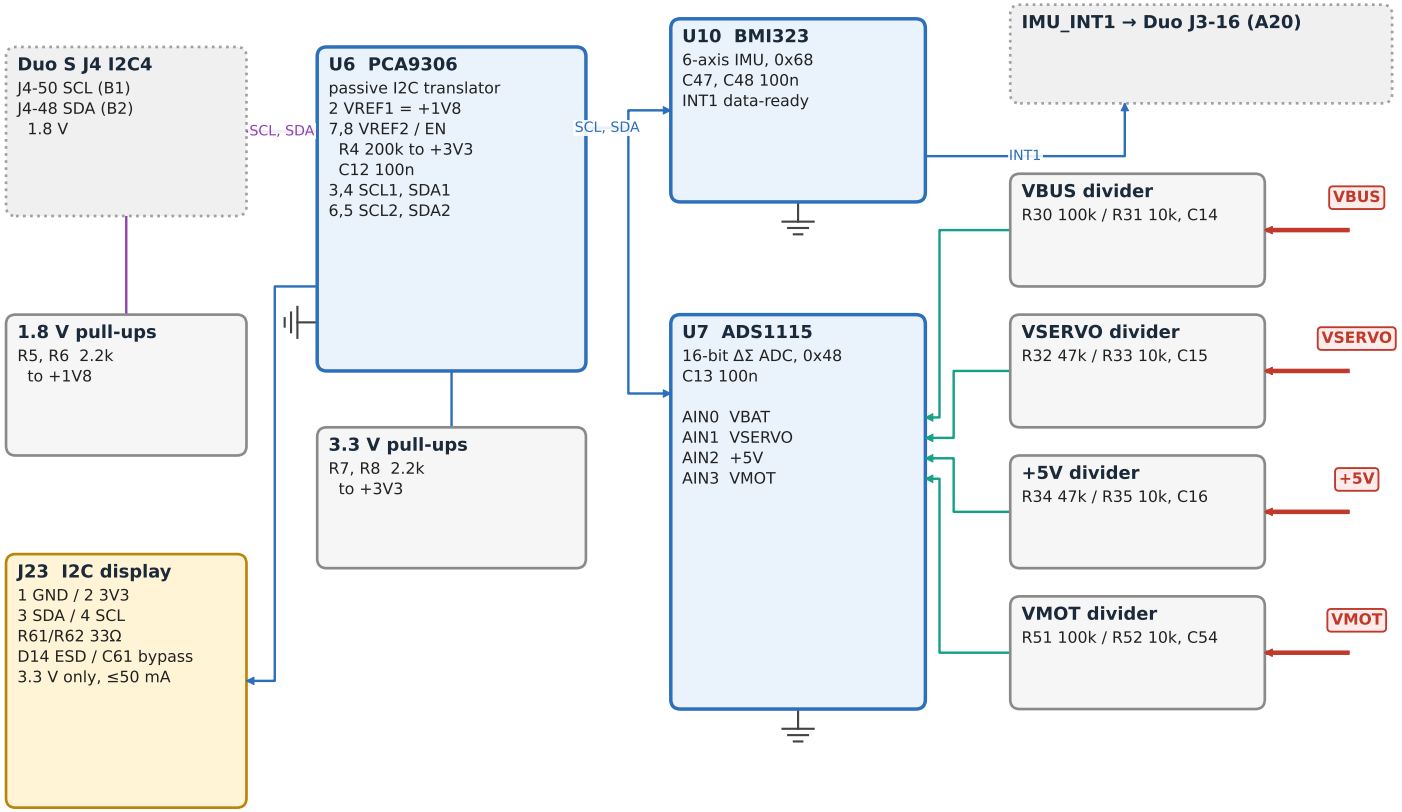
- The sensor cables run beside the motor phase leads, hence an SP0504BAHT array (5.5 V standoff) at every connector.
- SCK and MOSI are a star from R13/R14 to the four connectors, so every cable is a stub: keep the sensor cables short.
- F.Cu references In1 GND; B.Cu references logic 3V3 or the lower GND strip. C62–C71/C73–C75 provide local AC return transfer; review the complete capacitor/via loops and measure the assembled harness.

Layout check (measured on the routed board)

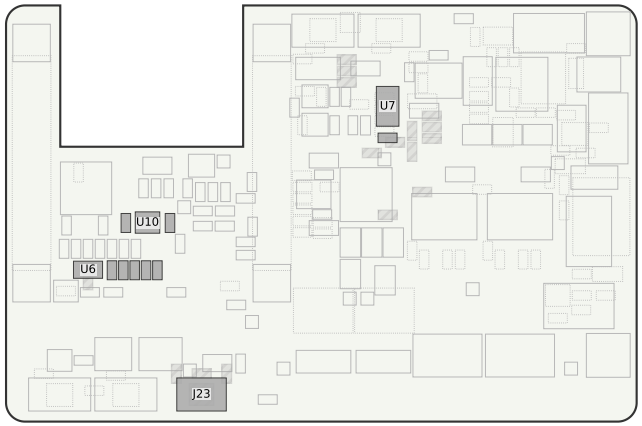
OK	SPI_SCK: 0.2 of 219 mm without a plane under it (fast edges)
CHECK	SPI_MOSI: 1.6 of 165 mm without a plane under it (fast edges)
CHECK	SPI_MISO: 3.8 of 117 mm without a plane under it (fast edges)
CHECK	CS_ROTOR_R: 2.8 of 30 mm without a plane under it (fast edges)
CHECK	CS_KNEE_L: 4.6 of 55 mm without a plane under it (fast edges)
CHECK	SPI_SCK routed 219 mm with 8 vias to four connectors
CHECK	191 of 501 mm of SCK/MOSI/MISO is on B.Cu. SPI autorouting is constrained to the outer layers. In1 is GND; In2 has logic 3V3, selected control routes and a stitched lower GND strip. Validate the complete four-cable harness under motor switching.
OK	SPI transition/header to nearest 3V3/GND capacitor: worst 5.07 mm (/CS_KNEE_L); target ≤5.08 mm. Geometry alone does not qualify the return loop.

S10 I2C4: IMU (BMI323) and rail monitor (ADS1115)

Duo S I2C4 is on the 1.8 V header. A PCA9306 passes it to a 3.3 V segment with the on-board BMI323 IMU (balance loop), ADS1115 rail monitor and optional 3.3 V display connector J23.



Where it is (top view; hatched = bottom side)



Layout check (measured on the routed board)

CHECK	U6 pin 2 (+1V8) to nearest GND bypass C7 (100n): 8.5 mm; keep ≤ 3 mm (VREF1 only biases the pass gates, so low priority)
OK	U10 pin 8 (+3V3) to nearest GND bypass C47 (100n): 2.2 mm; keep ≤ 3 mm
CHECK	U10 pin 12 (+3V3) to nearest GND bypass C47 (100n): 3.5 mm; keep ≤ 3 mm
OK	U7 pin 8 (+3V3) to nearest GND bypass C13 (100n): 3.0 mm; keep ≤ 3 mm
CHECK	I2C_SCL: 1.9 of 165 mm without a plane under it (slow signal)
OK	I2C_SDA_1V8: 0.6 of 64 mm without a plane under it (slow signal)

Derived values

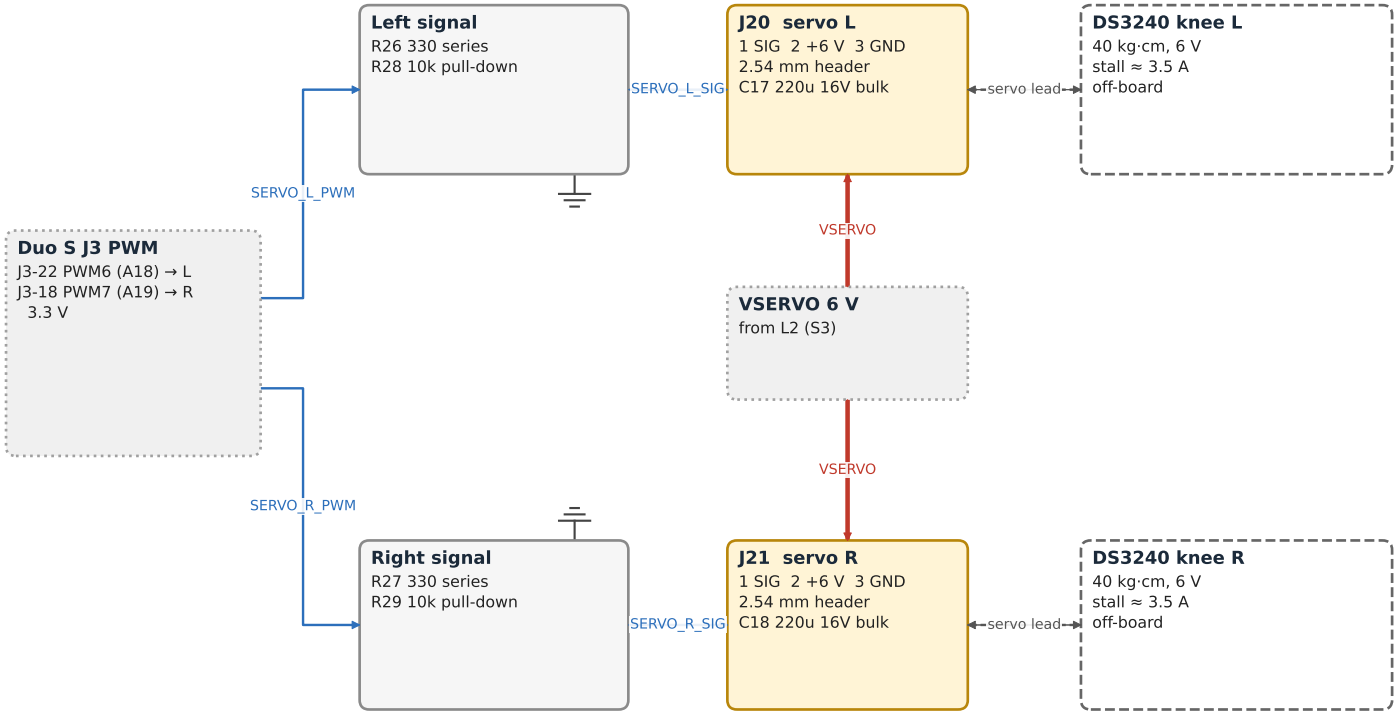
- Divider outputs at nominal: VBUS 1.53 V, VSERVO 1.05 V, +5V 0.93 V, VMOT 1.53 V; ADS1115 at ±2.048 V reads up to VBUS 22.5 V, VSERVO 11.7 V, +5V 11.7 V, VMOT 22.5 V.
- VBAT filter: (R30 ‖ R31) × C14 → fc ≈ 175 Hz, well above the monitor's sample rate.
- Pull-ups 2.2k: rise time 0.85·R·C ≈ 94 ns at 50 pF, inside fast-mode's 300 ns.

Notes

- J23 shares the IMU bus: use low-priority short display transfers and preserve IMU deadlines. Do not hot-plug; a stuck external device can hold the bus low.
- BMI323 is 0x68 and ADS1115 0x48. Match the display address; all pull-ups must go to 3.3 V. Verify 400-kHz rise time with the actual cable/display.
- U6 is a pass-gate translator: pull-ups are needed on both sides (R5/R6 and R7/R8).

S11 Knee servos: 2 × DS3240 on the 6 V rail

Two hobby-servo headers carry VSERVO, GND and a conditioned PWM signal from Duo S PWM6/7 (50–330 Hz). Each header has its own 220 µF bulk capacitor for the servo's current pulses.



Where it is (top view; hatched = bottom side)



Layout check (measured on the routed board)

- OK — VSERVO: 10 vias into the In2 VSERVO region
- CHECK — SERVO_L_SIG: 12.7 of 80 mm without a plane under it (slow signal)
- CHECK — SERVO_R_SIG: 3.6 of 97 mm without a plane under it (slow signal)

Derived values

- Series 330 Ω: a servo lead shorted to 6 V pushes at most (6 − 3.3) V / 330 Ω ≈ 8 mA into the Duo pin's clamp.
- Pull-down 10k: no pulses, so the servo idles while the Duo S boots.
- Two stalls ≈ 7 A from the 8 A buck; the 220 µF at each header covers the servo's inrush pulses.

Notes

- PWM6/7 on A18/A19 are also the little core's JTAG TCK/TMS: JTAG is not available with servos fitted.
- The knee angle is measured, not commanded: the AS5048A boards on the knee axes are in S9.

S12 Duo S interface, debug UART and mechanics

The carrier plugs onto a stock Milk-V Duo S with two 2×13 sockets on its bottom side. J8 takes Duo header J3 (3.3 V logic), J9 takes J4 (1.8 V logic). Pins below are coloured by the subsystem that uses them.

J8 ← Duo S J3 (3.3 V)

1	—	2	VSYS
3	MR_IN3	4	VSYS
5	CS_KNEE_R	6	GND
7	CS_ROTOR_R	8	CON_TX
9	—	10	CON_RX
11	MR_IN1	12	MOT_EN_REQ
13	MR_IN2	14	GND
15	CS_KNEE_L	16	IMU_INT1
17	—	18	SERVO_R_PWM
19	SPI_MOSI_RAW	20	GND
21	SPI_MISO	22	SERVO_L_PWM
23	SPI_SCK_RAW	24	CS_ROTOR_L
25	GND	26	DRV_NFAULT

J9 ← Duo S J4 (1.8 V)

27	—	28	—
29	—	30	—
31	GND	32	GND
33	—	34	—
35	—	36	ESTOP_ARM_1V8
37	GND	38	GND
39	DRV_NSLEEP_1V8	40	ML_IN1_1V8
41	DRV_NRESET_1V8	42	ML_IN2_1V8
43	—	44	ML_IN3_1V8
45	—	46	WDT_KICK_1V8
47	—	48	I2C_SDA_1V8
49	—	50	I2C_SCL_1V8
51	—	52	VSYS

CON_TX, CON_RX (J3-8, J3-10)

J22 debug UART0
JST-SH 3-pin
1 GND
2 TX ← J3-8 (A16)
3 RX → J3-10 (A17)

Test points
TP3/4/11 GND
TP5 VBUS / TP6 VMOT
TP7 6V / TP8 5V
TP9 RUN / TP10 FAULT

Mounting
H1, H2 M3 chassis
H5–H8 M2.5 Duo S standoffs
carrier ≈ 11 mm above the Duo S

Where it is (top view; hatched = bottom side)



Layout check (measured on the routed board)

- CHECK CON_TX: 6.0 of 66 mm without a plane under it (slow signal)
- CHECK CON_RX: 5.5 of 155 mm without a plane under it (slow signal)

Derived values

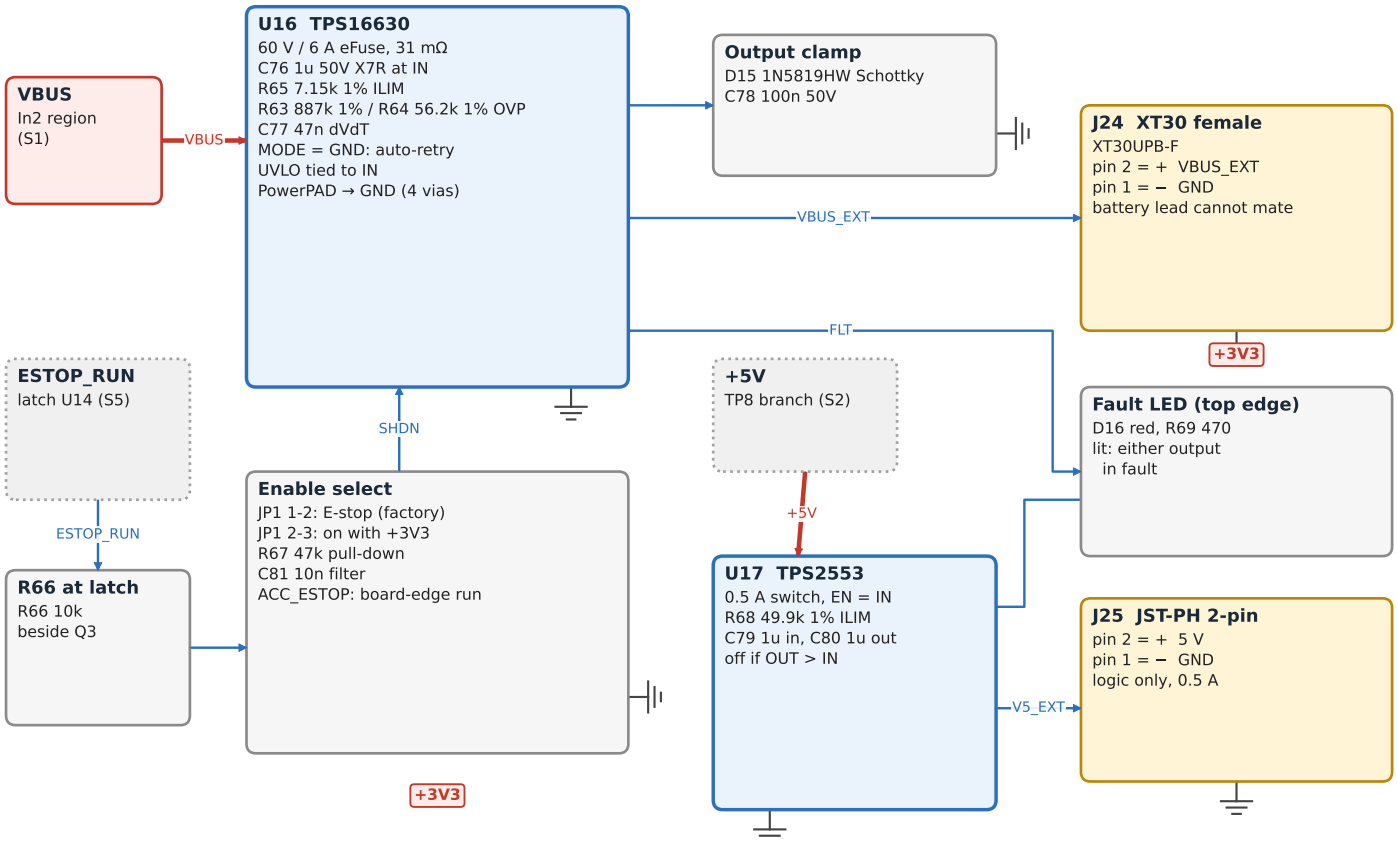
- Used pads: J8 19 nets, J9 11 nets (GND and VSYS counted once).
- VSYS reaches the Duo on J3-2, J3-4 and J4-52 from D3 (S4).
- generate_pcb.py fails the build if a socket pad is not exactly on its Duo S pin (Milk-V DUO_S_MB_V1_2-TOP.dxf).

Notes

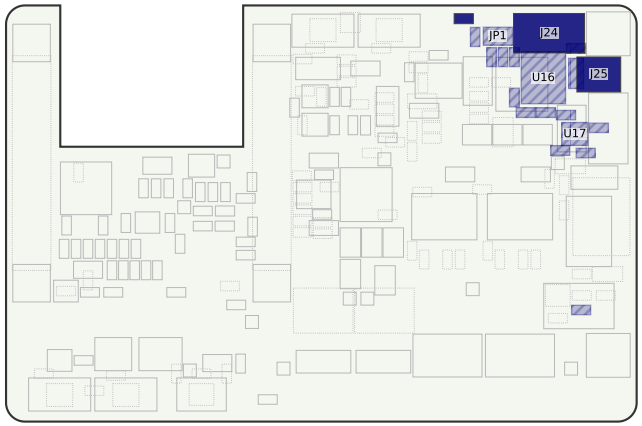
- Left free: J3-9 (GPIO on Duo S v1.1, GND on v1.2+), the Duo's own 3V3 pins, J4-45/47/49/51 (audio pads) and the J4 MIPI pins.
- UART0 is the Linux console; there is no other free UART (A18/A19 and B11/B12 are PWM, J4's UART shares I2C4).
- Linux must not claim I2C4, SPI3, PWM controllers 0–2 or any of these pads.

S13 Accessory power outputs: VBUS eFuse (J24) and 5 V switch (J25)

Two outputs for devices off the carrier, such as an accessory MCU and an arm. J24 gives the protected battery voltage through a current-limited eFuse that follows the E-stop by default; J25 gives the 5 V logic rail through a current-limited switch that blocks back-feed.



Where it is (top view; hatched = bottom side)



Derived values

- I(OL) = 18 / R65[kΩ] = 2.52 A (±7 %), fast trip at 2 × I(OL); after about 162 ms in current limit the eFuse turns off and auto-retries.
- OVP = 1.2 V × (R63 + R64)/R64 = 20.1 V, between the 16.8 V full pack and the 32 V TVS clamp.
- Output slew = 1/(20.8 kΩ × C77) = 1.02 V/ms: about 0.48 A into 470 µF, 16.8 V reached in 16 ms.
- SHDN driven high: 3.3 V × R67/(R66 + R67) = 2.72 V (on above 2 V). With U14 unpowered, the pin's 10 µA lifts ESTOP_RUN to at most 0.30 V, below Q3's threshold.
- U17 limit: 23950 / R68[kΩ]^0.977 = 525 mA typical (475–565 mA).
- Fault LED: (3.3 − 2.0) V / 470 Ω ≈ 2.8 mA.

Notes

- Factory default: J24 follows the E-stop latch, so an open loop removes the arm supply with the motor supply. To keep it on, cut JP1 1-2 and bridge 2-3.
- J25 is logic power only and stays on. Power servos from J24 through an external converter rated for at least 35 V in.
- VBUS_EXT can reach 20 V during regeneration before OVP opens. No ADC channel monitors either output.
- ACC_ESTOP is 10k-isolated from ESTOP_RUN and runs round the right and top board edges; C81 filters it.

Layout check (measured on the routed board)

OK	OUT → J24.2 (VBUS_EXT): 0.9 mm path ≈ 3.0 A (IPC-2221, 20 °C rise); needs 2.5 A. The 0.5–0.6 mm branches to C78/D15 carry only transients.
OK	U17 → J25 (V5_EXT): narrowest 0.5 mm over 10.4 mm carries ≈2.0 A (IPC-2221, 1 oz outer, 20 °C rise); needs 0.5 A
CHECK	U16 pin 1 (VBUS) to nearest GND bypass C76 (1u 50V X7R): 3.2 mm; keep ≤ 3 mm; C76 sits below the VBUS vias
OK	U17 pin 1 (+5V) to nearest GND bypass C79 (1u): 2.6 mm; keep ≤ 3 mm
OK	U16 PowerPAD: 4 GND vias (TI: solder it to the GND plane)
OK	ACC_ESTOP: 0.0 of 83 mm without a plane under it (slow signal)
CHECK	ACC_ESTOP: 83 mm, 2 vias round the board edge. Scope SHDN while the motors switch before relying on it.